Ch.2 Data Storage

Semiconductor Basic Memories

- **Memory** is a device that stores binary data as a byte, word, double word, etc.
- Addressing is the process of accessing a specified location in memory. The **write** operation puts data into a specified address, and the **read** operation copies data out of a specified address in the memory.
- Figure 2-1 shows the address bus, address decoder, bidirectional data bus and read/write inputs.
- Figures 2-2 and 2-3 show the write and read operation in the memory.
- In personal computers a 32-bit address bus can select 4,294,296 locations (2^{32}), expressed as 4G.
- The two major categories of memories are the random-access memory (RAM) and the read only memory (ROM).
- RAMs are volatile and ROMs are nonvolatile.

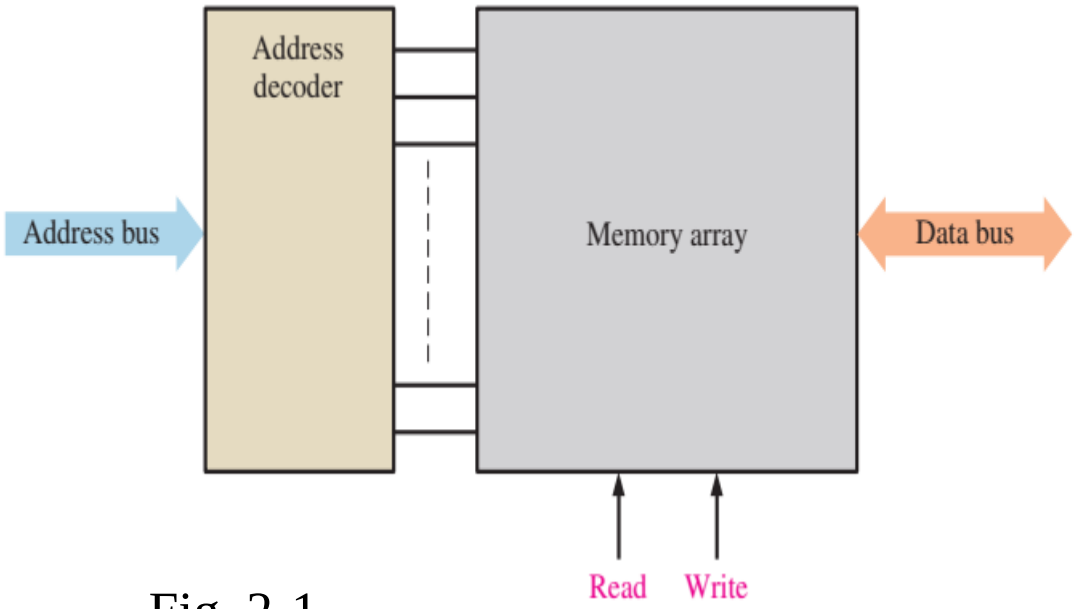
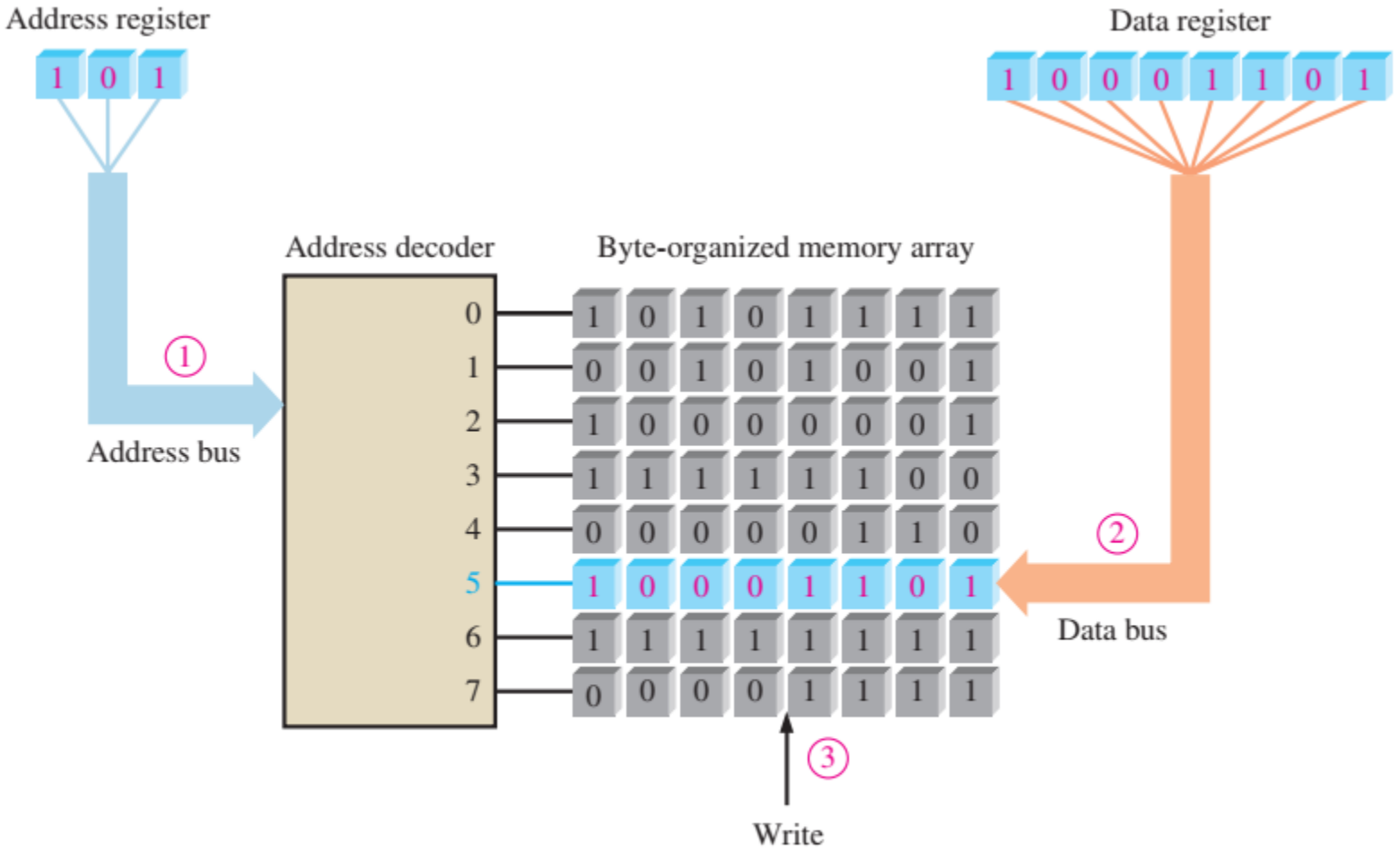
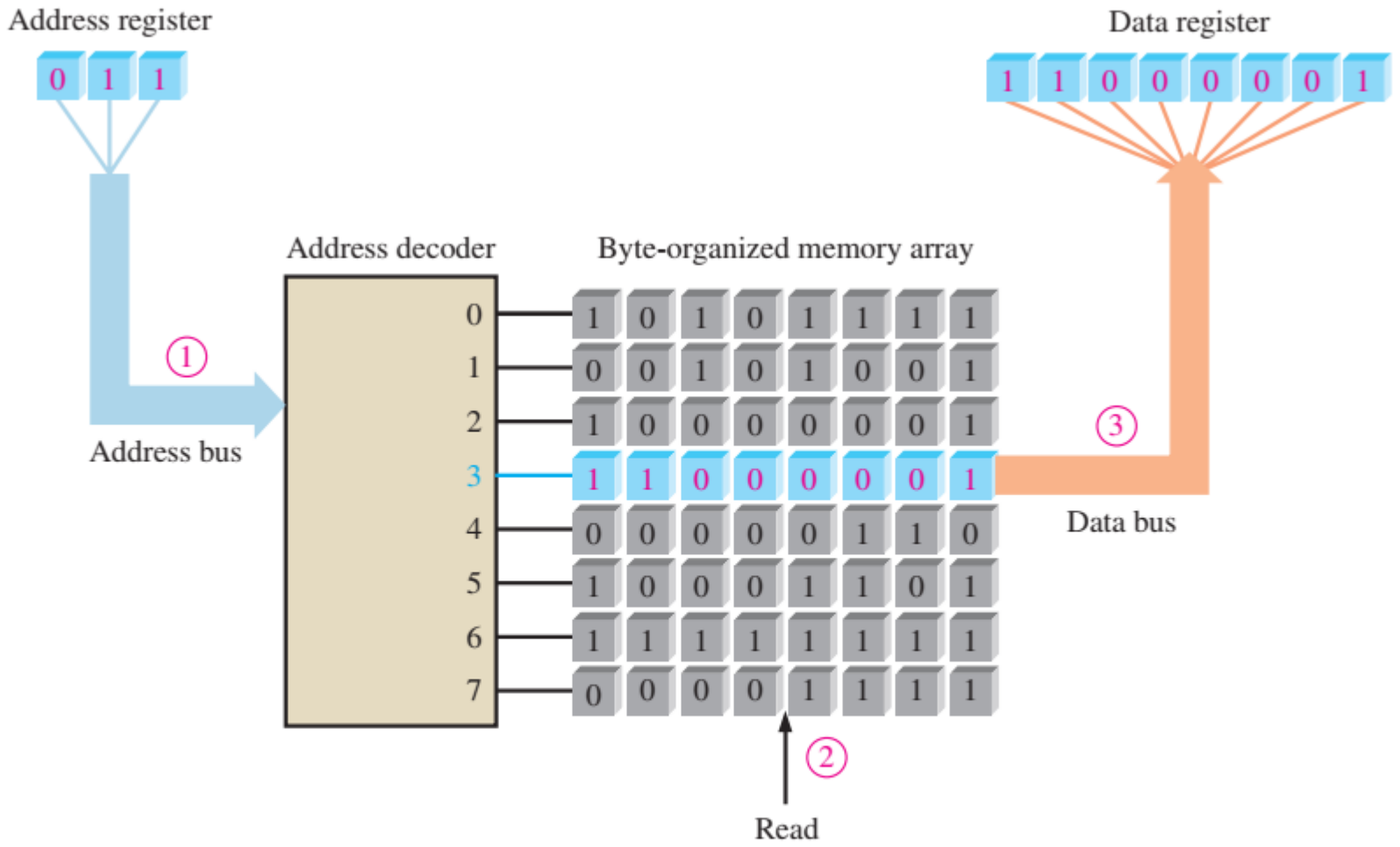


Fig. 2-1



1. Address code 101 is placed on the address bus and address 5 is selected.
2. Data byte is placed on the data bus.
3. Write command causes the data byte to be stored in address 5, replacing previous data.

Fig. 2-2 Write operation



1. Address code 011 is placed on the address bus and address 3 is selected.
2. Read command is applied.
3. The contents of address 3 is placed on the data bus and shifted into data register. The contents of address 3 is not erased by the read operation.

Fig. 2-3 Read operation

The RAM Family

Figure 2-4 shows the RAM family.

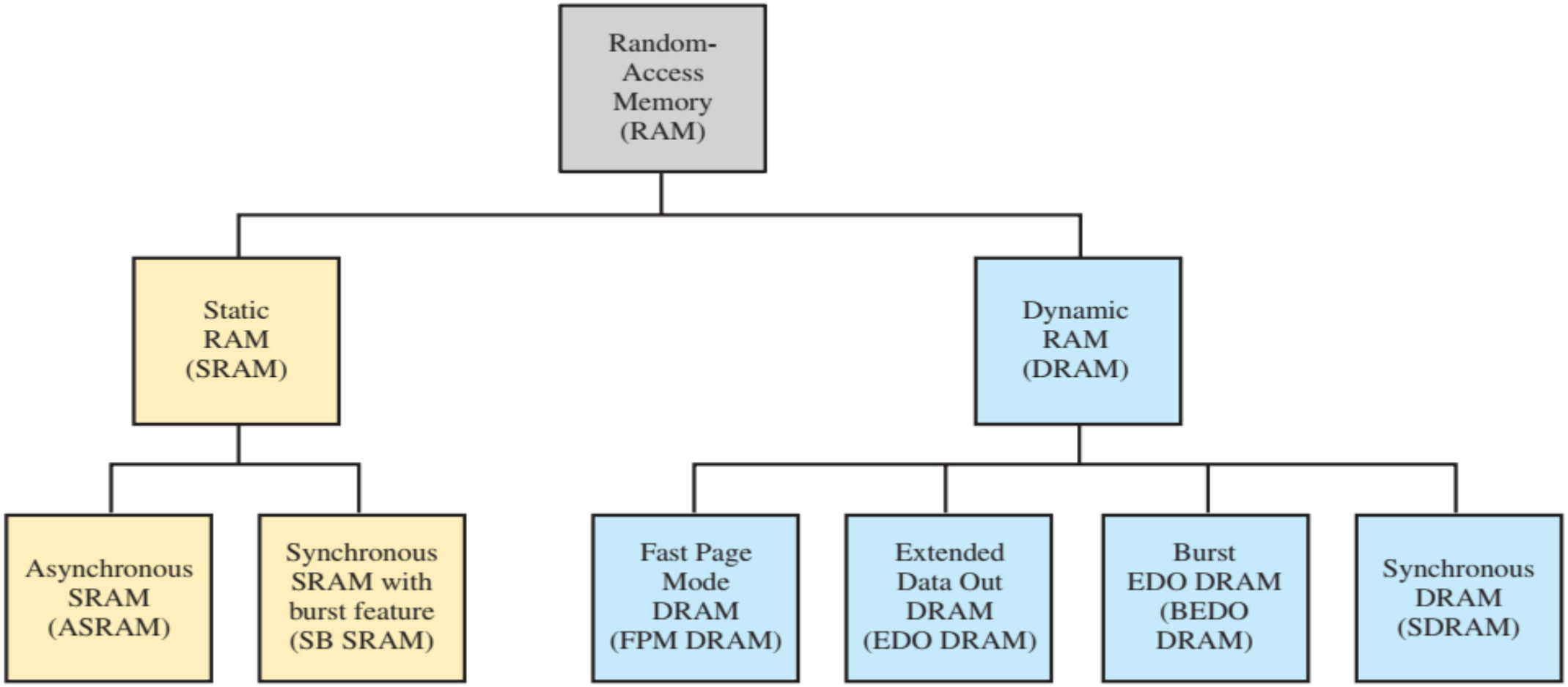
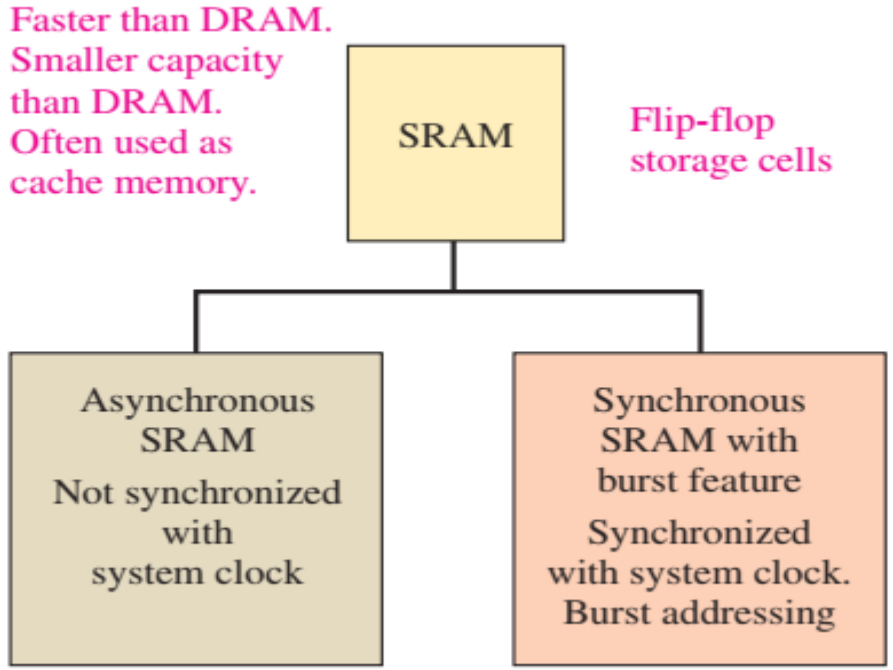


Fig. 2-4 RAM family.

Static RAMs (SRAMs)

- All SRAMs are characterized by latch memory cells. As long as dc power is applied to a SRAM cell, it can retain a 1 or 0 state. If power is removed, the stored data bit is lost.
- Figure 2-5 shows a basic SRAM latch memory cell.



Static Memory Cell Array

- The memory cells in a SRAM are organized in rows and columns, as shown in Fig. 2-6.

Asynchronous SRAM Organization

- An asynchronous SRAM is one in which the operation is not synchronized with a system clock.
- Figure 2-7 shows a logic symbol for a 32k x 8 bit SRAM memory.

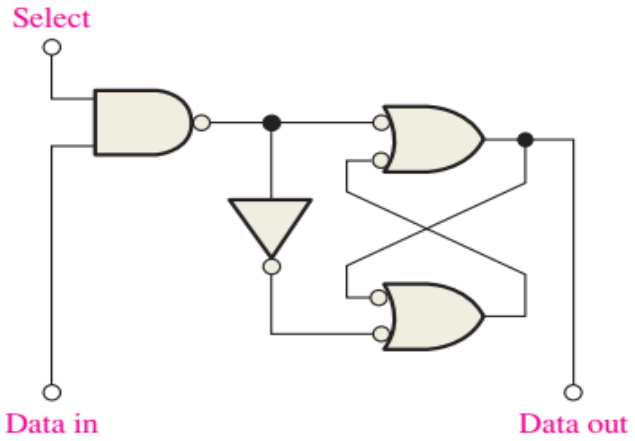


Fig. 2-5 A SRAM cell.

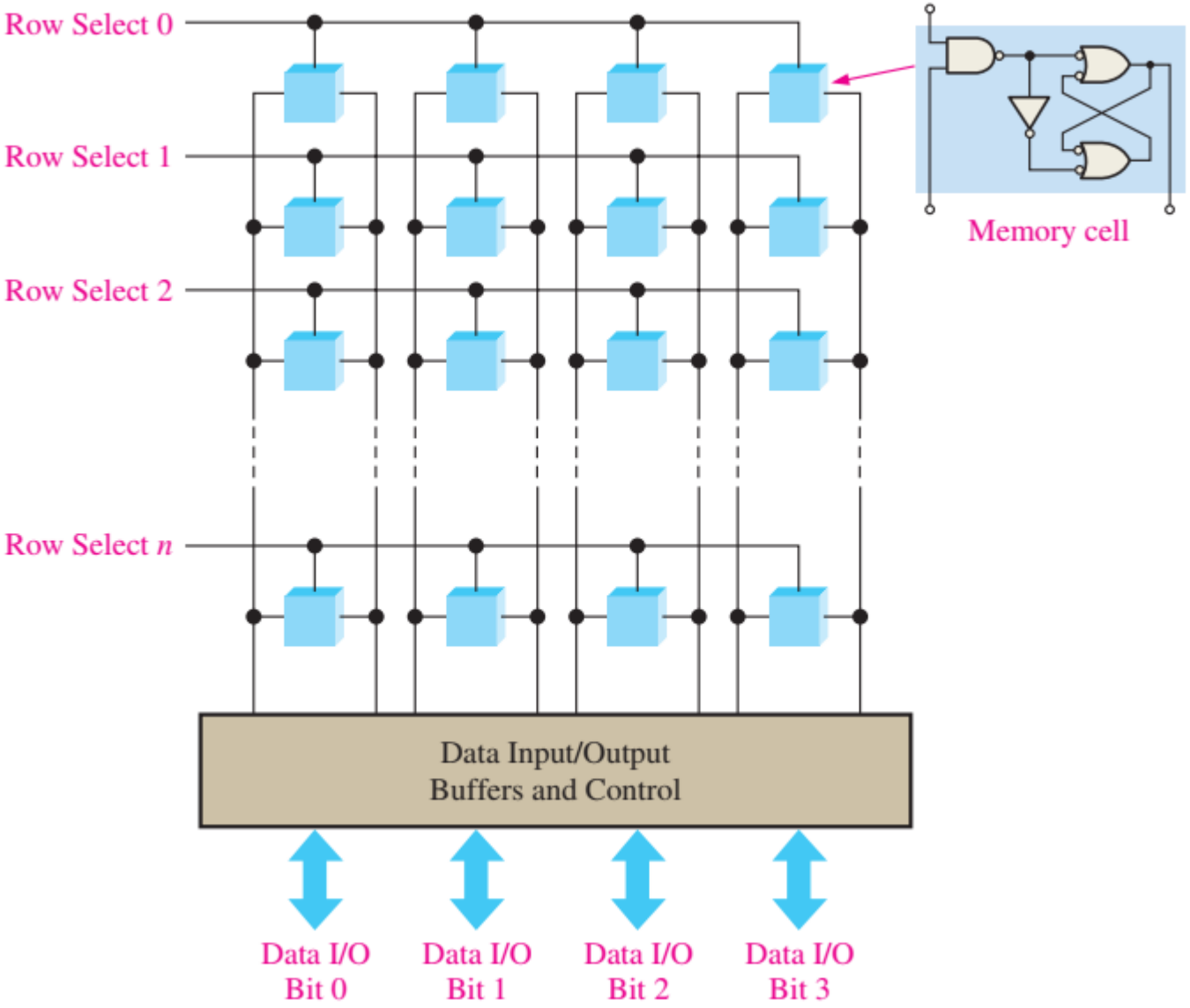


Fig. 2-6 Basic SRAM array.

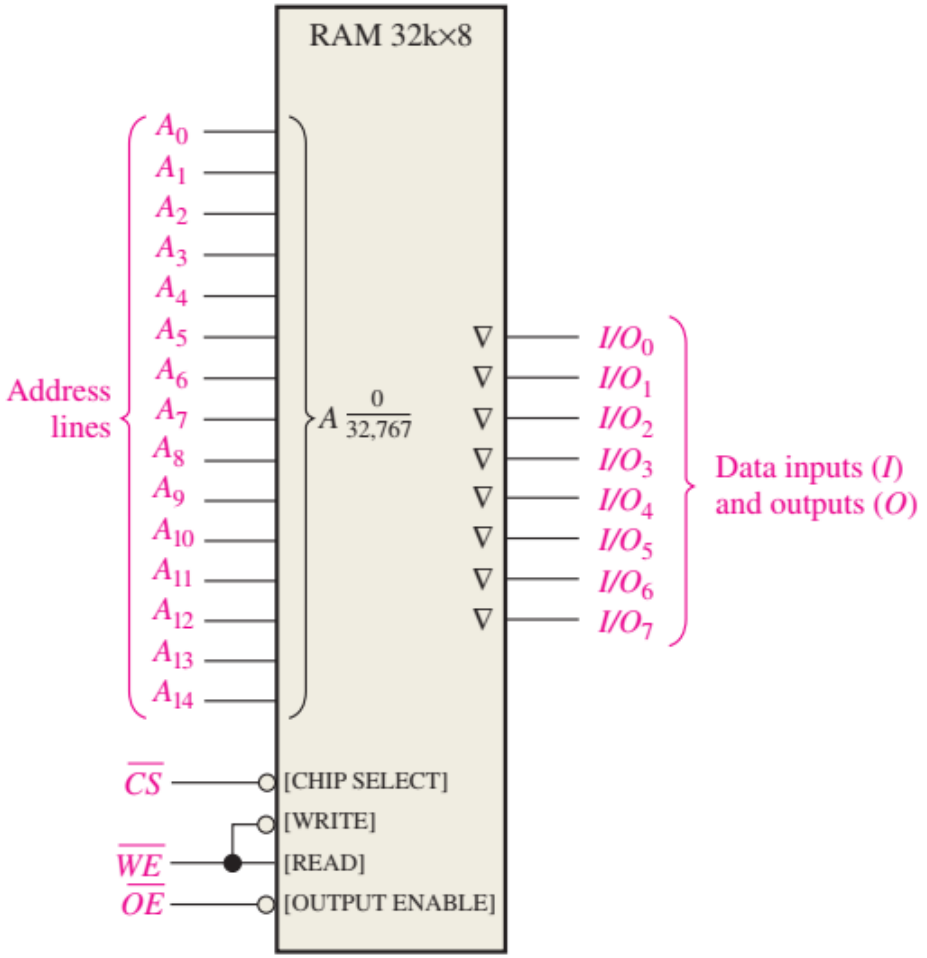


Fig. 2-7 Logic diagram for an asynchronous 32k X 8 SRAM.

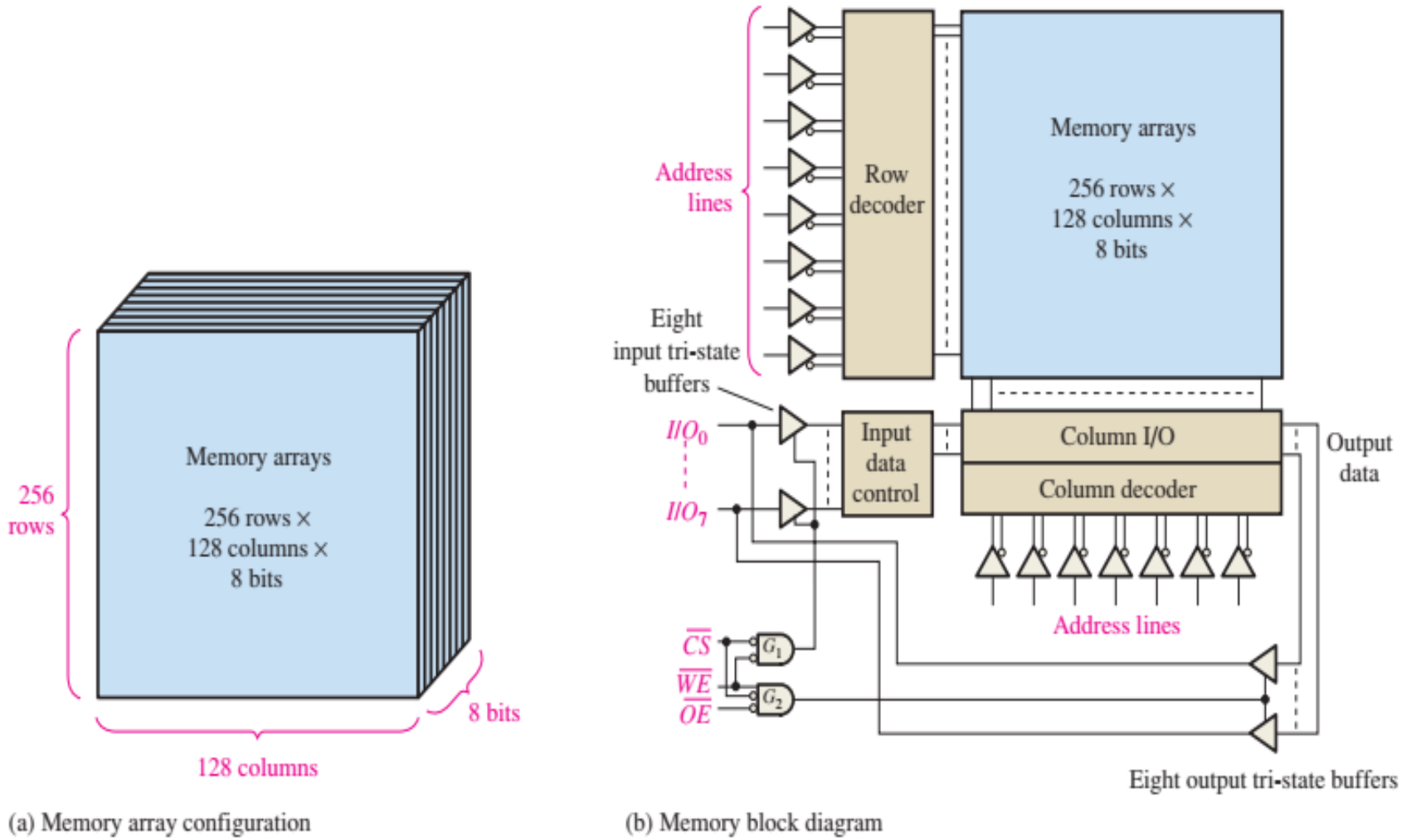


Fig. 2-8 Basic organization of an asynchronous 32k x 8 SRAM.

Read and Write Cycles

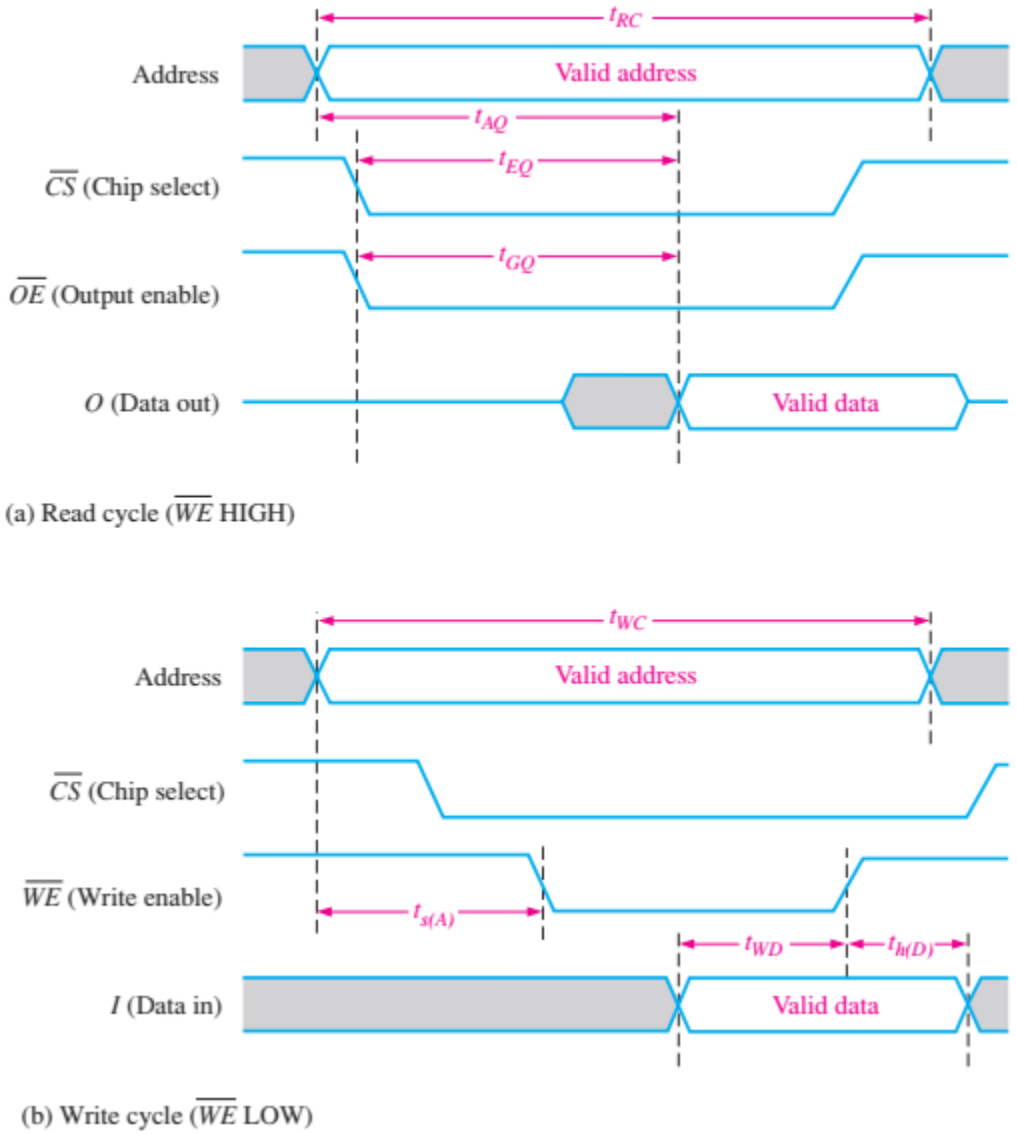


Fig. 2-9 Timing diagrams for typical read and write cycles for the SRAM in Fig. 2-8.

Synchronous SRAM with Burst Feature

- A synchronous SRAM is synchronized with the system clock.

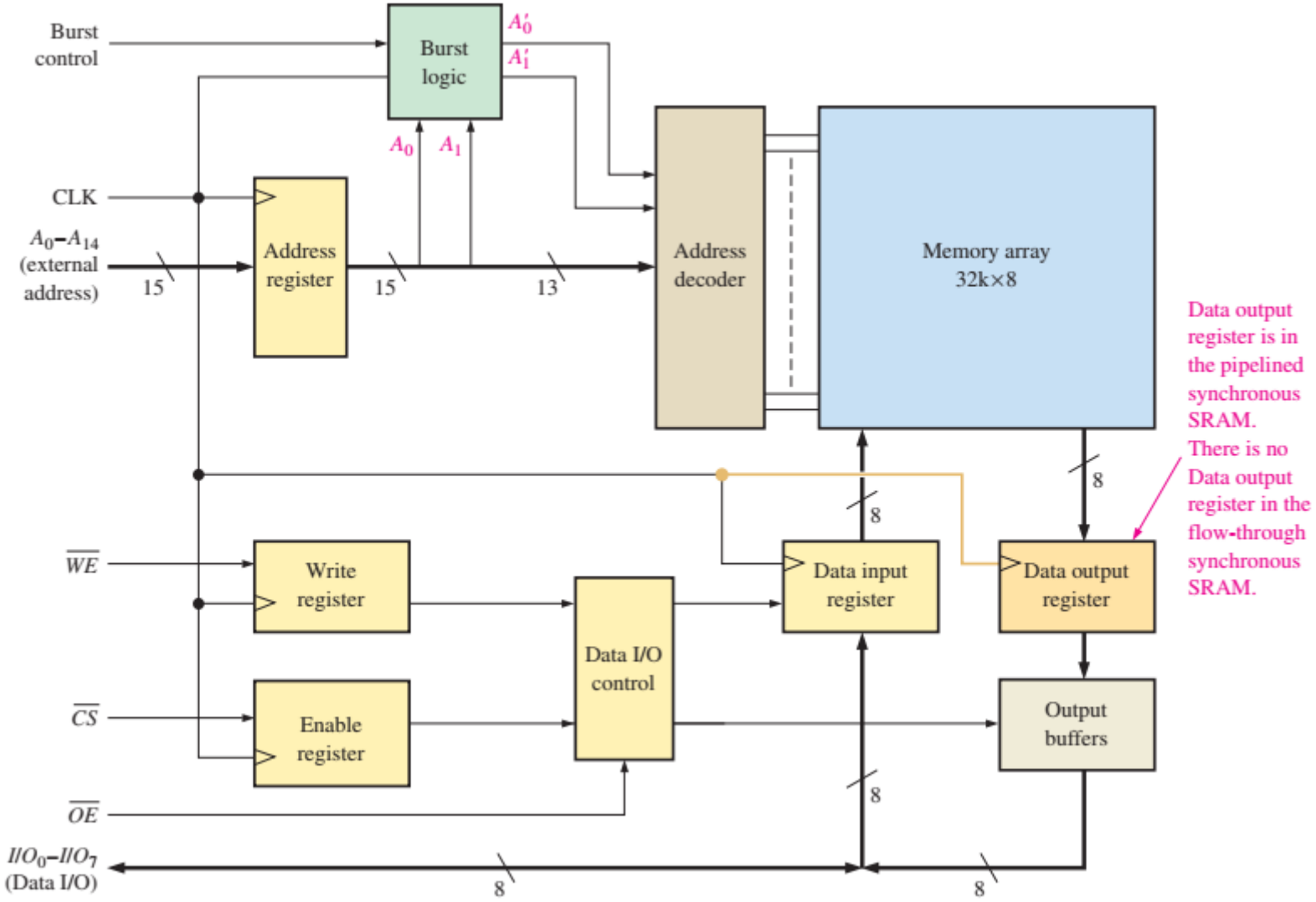


Fig. 2-10 a basic block diagram of a synchronous SRAM with burst feature.

The Burst Feature

- The address burst feature allows the memory to read or write up to four sequential locations using a single address.
- When an external address is latched in the address register, the two lowest-order address bits, A_0 and A_1, are applied to the burst logic. This produces a sequence of four internal addresses by adding 00, 01, 10, and 11 to the two lowest-order address bits on successive clock pulses.
- The address burst logic consists of a binary counter and exclusive-OR gates as shown in Fig. 2-11.

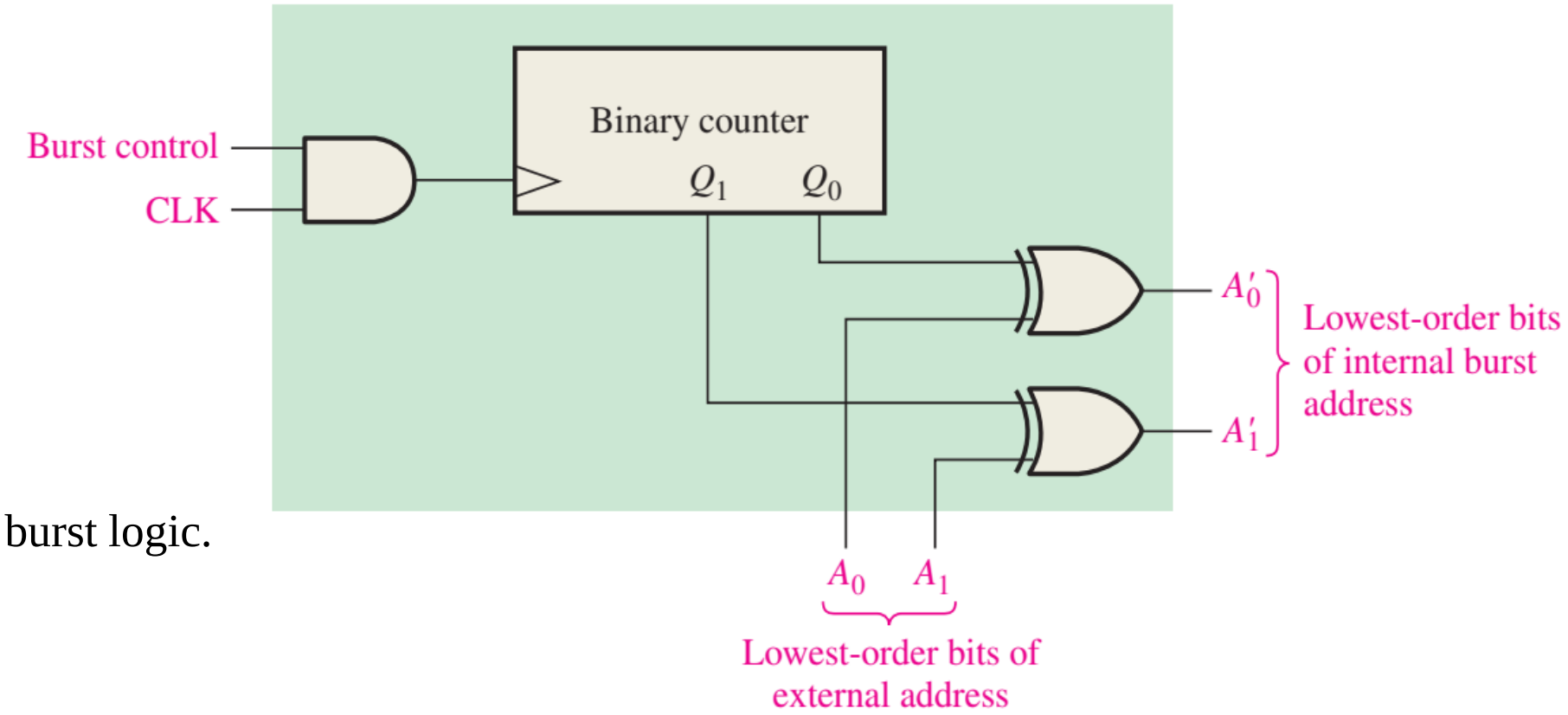


Fig. 2-11 Address burst logic.

Cache Memory

- One of major applications of SRAMs is in cache memories in computers.
- Cache memory is relatively small, high speed but slower than the main memory.
- A first level cache (L1 cache) is usually integrated into the processor chip and has a very limited storage capacity.
- A second level cache (L2 cache) may also be integrated into the processor or as a separate memory chip or set of chips external to the processor; it is usually has a larger storage capacity than an L1 cache.
- Figure 2-12 shows L1 and L2 cache memories in a computer system.

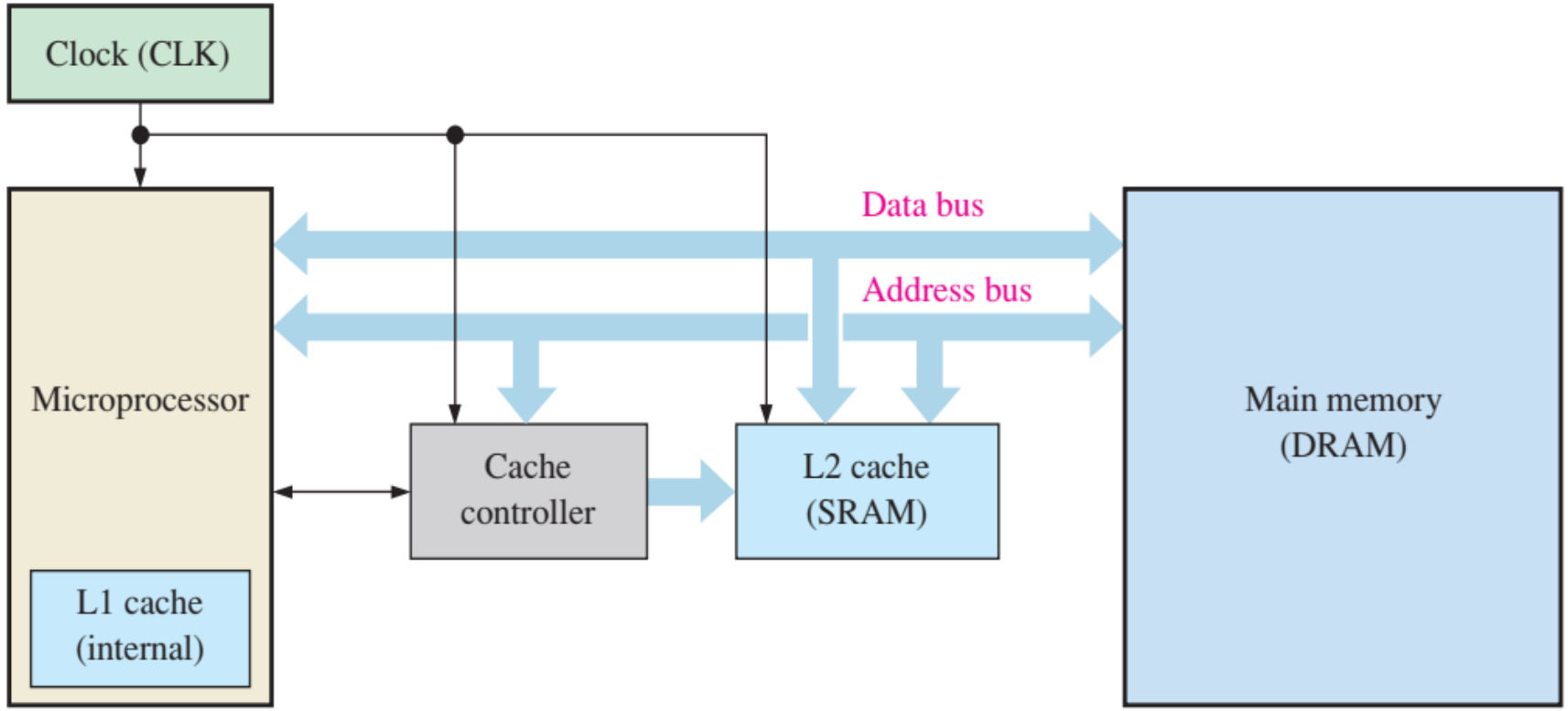


Figure 2-12 L1 and L2 cache memories.

Dynamic RAM (DRAM) Memory Cells

- Dynamic memory cells store a data bit in a small capacitor rather than in a latch.
- **Advantages:** very simple, lower cost per bit (very large arrays).
- **Disadvantages:** storage capacitor will lose the stored data bit unless its charge is refreshed periodically.
- Figure 2-13 shows a DRAM cell.
- Figure 2-14 shows a DRAM basic operation.

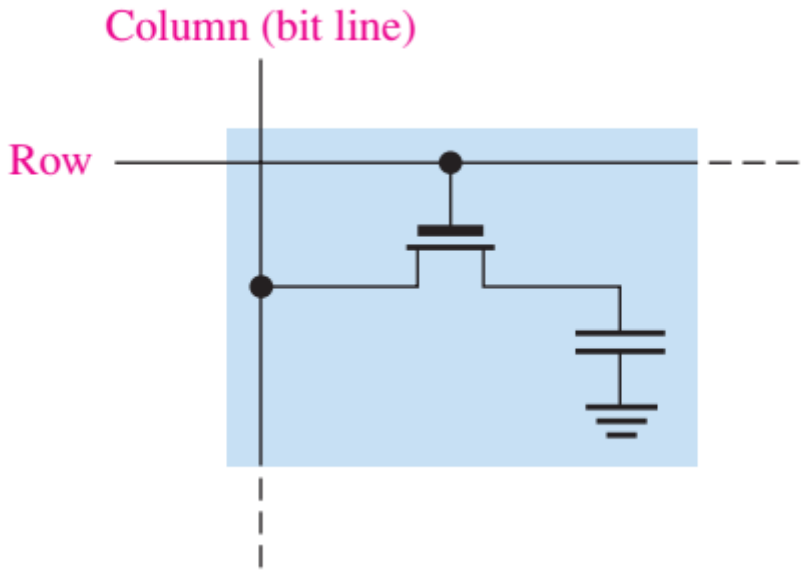
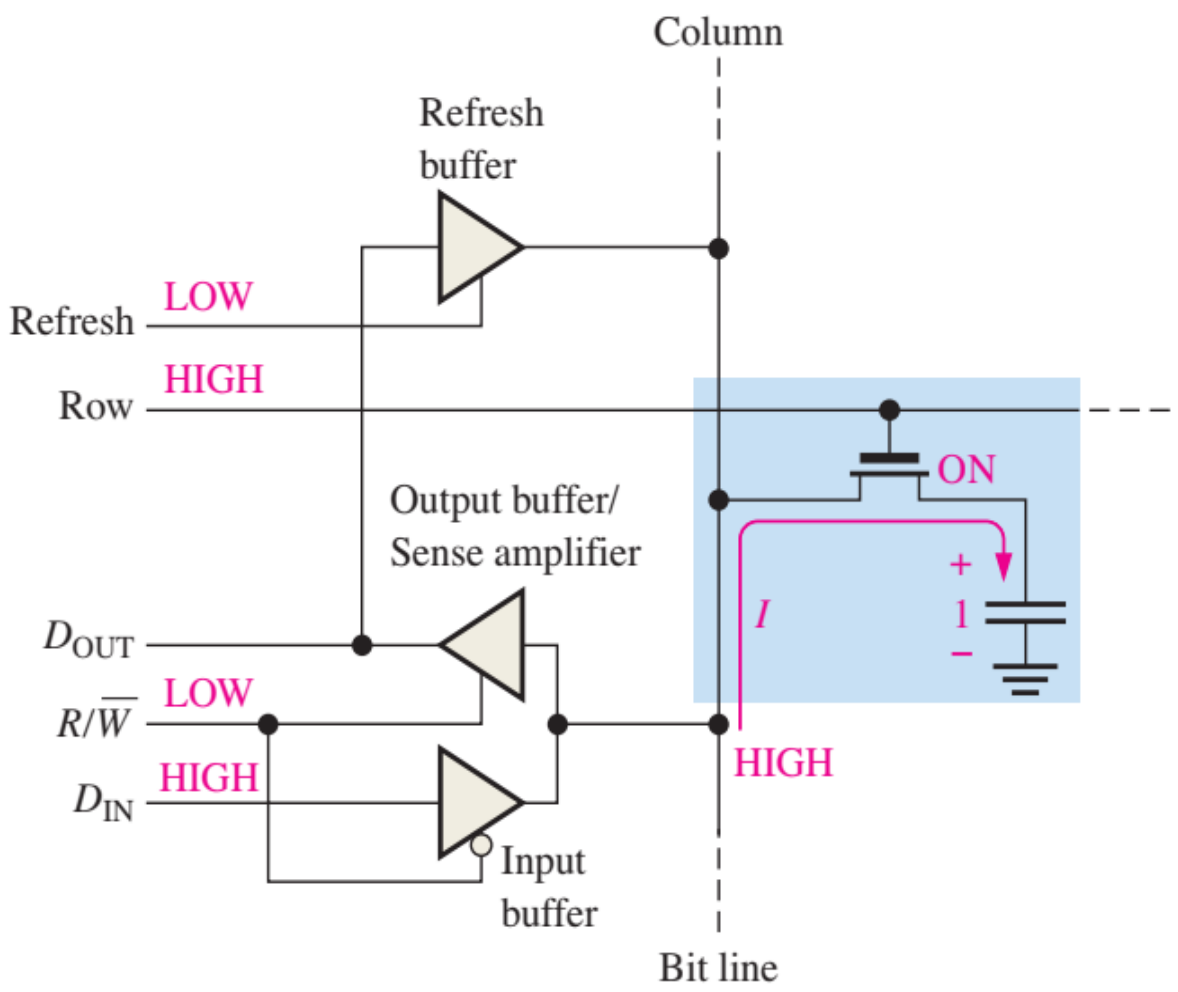
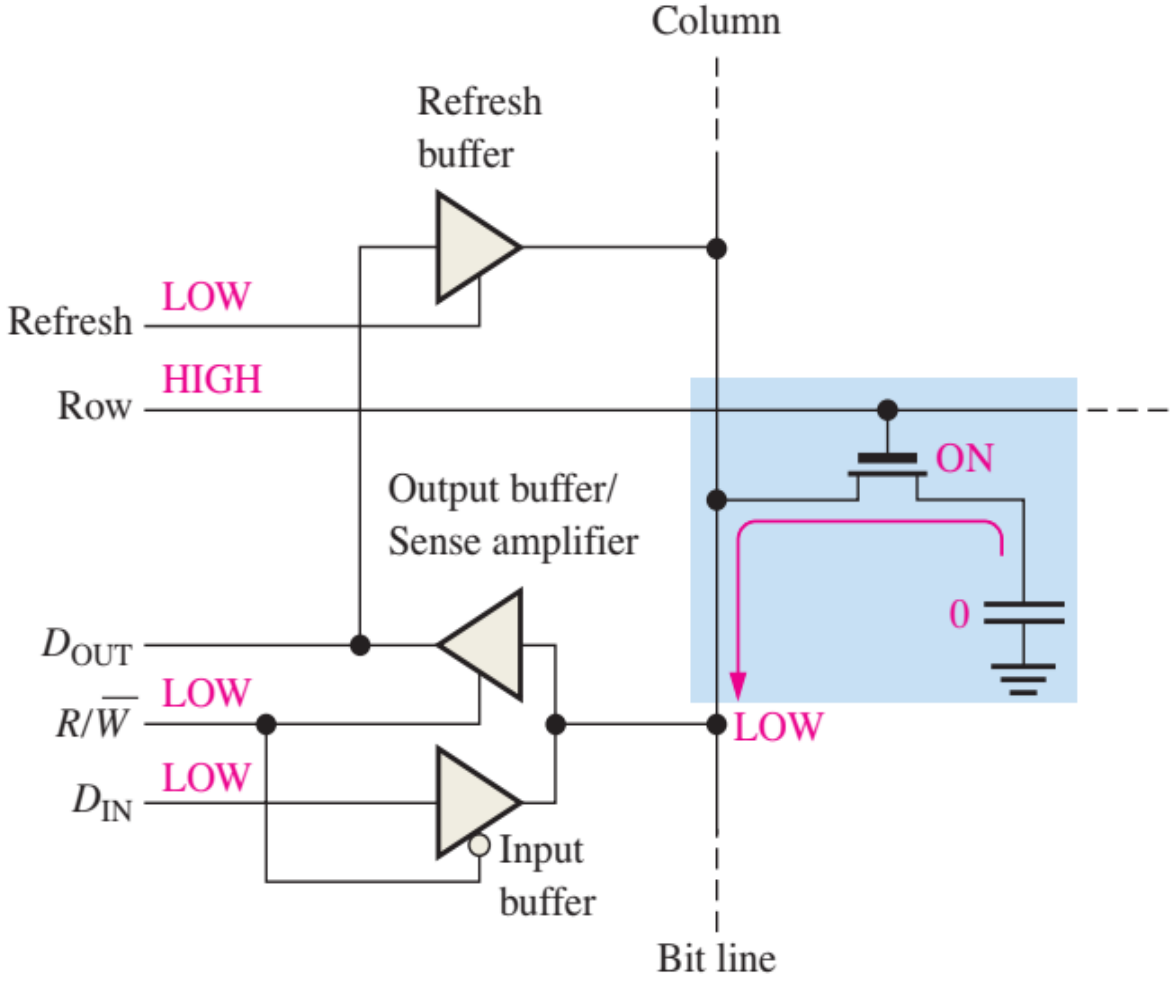


Figure 2-13 A MOS DRAM cell.

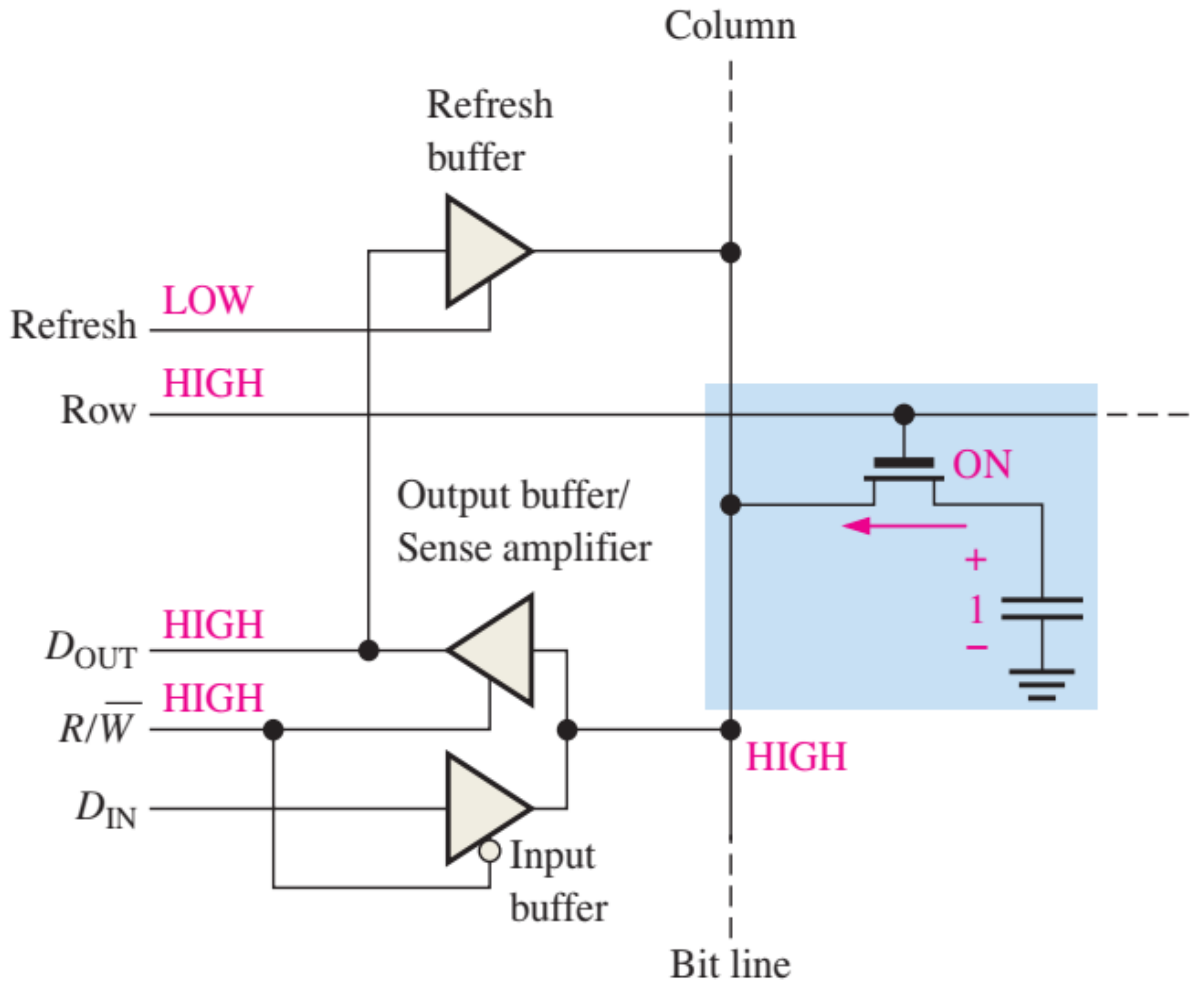


(a) Writing a 1 into the memory cell

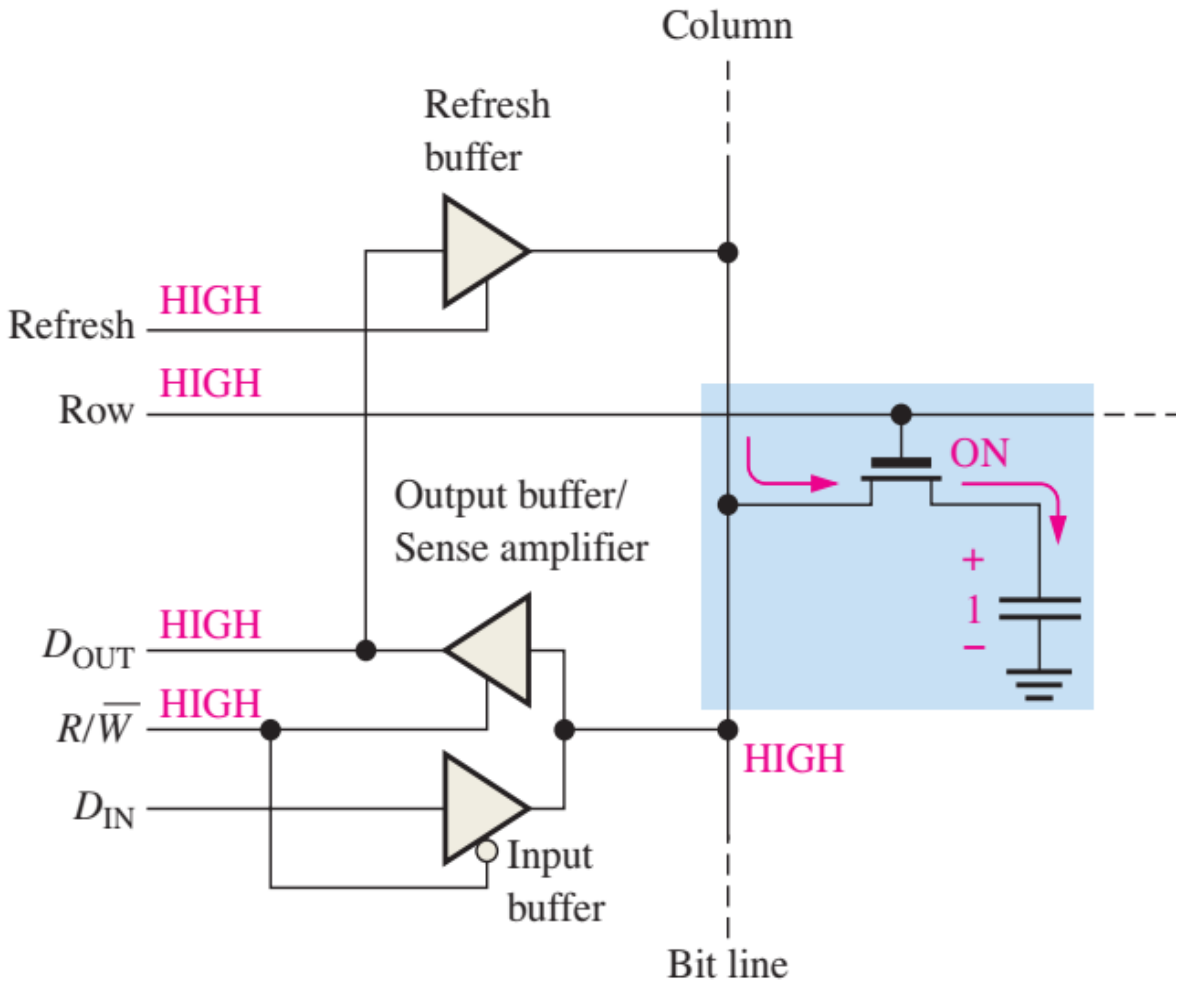


(b) Writing a 0 into the memory cell

Figure 2-14 Basic operation of a DRAM cell.



(c) Reading a 1 from the memory cell



(d) Refreshing a stored 1

Figure 2-14 Continued.

Read and Write Cycles

- At the beginning of each read or write memory cycles, $\overline{RAS}$ and $\overline{CAS}$ go active LOW to multiplex the row and column addresses into the registers, and decoders. For read cycle, the $R/\overline{W}$ input is HIGH. For a write cycle, the $R/\overline{W}$ input is LOW. This is indicated in Fig. 2-15.
- Figure 2-16 shows the simplified block diagram of a 1M x 1 DRAM.

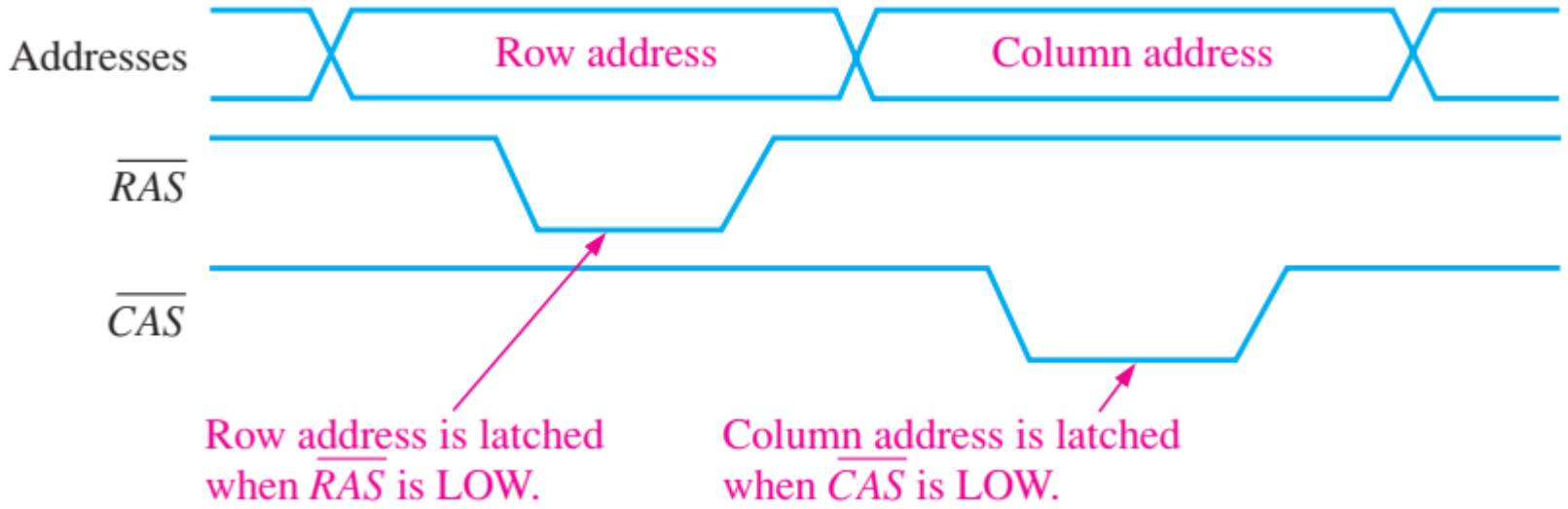


Figure 2-15 Basic timing for address multiplexing.

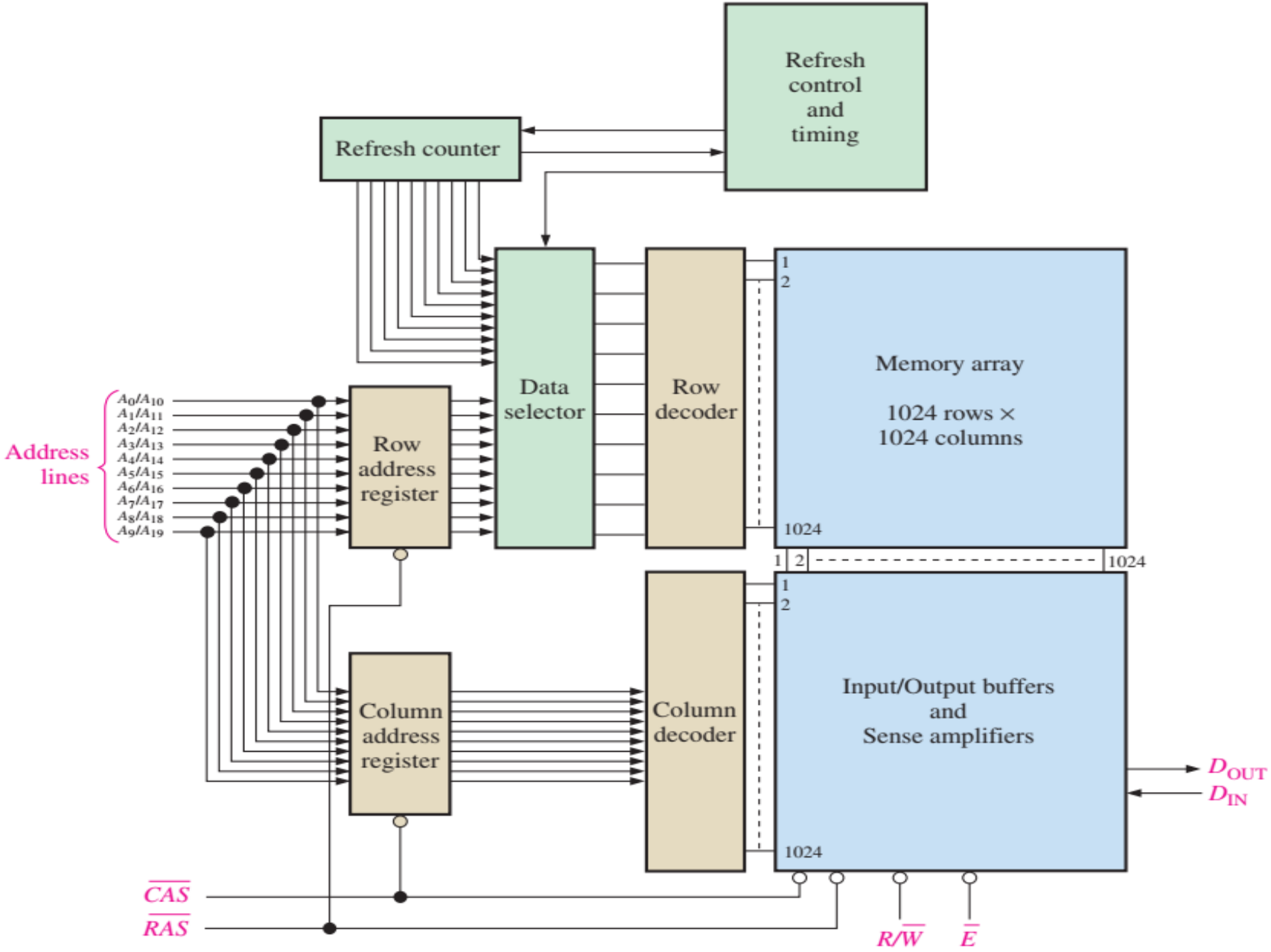

Refresh control and timing
Refresh counter
Data selector
Row decoder
Memory array
1024 rows × 1024 columns
1
2
1024
Address lines
A_0/A_{10}
A_1/A_{11}
A_2/A_{12}
A_3/A_{13}
A_4/A_{14}
A_5/A_{15}
A_6/A_{16}
A_7/A_{17}
A_8/A_{18}
A_9/A_{19}
Row address register
Column address register
Column decoder
Input/Output buffers and Sense amplifiers
D_{OUT}
D_{IN}
$\overline{CAS}$
$\overline{RAS}$
$R/\overline{W}$
$\overline{E}$

Figure 2-16

Types of DRAMs

Figure 2-17 illustrates the DRAM types.

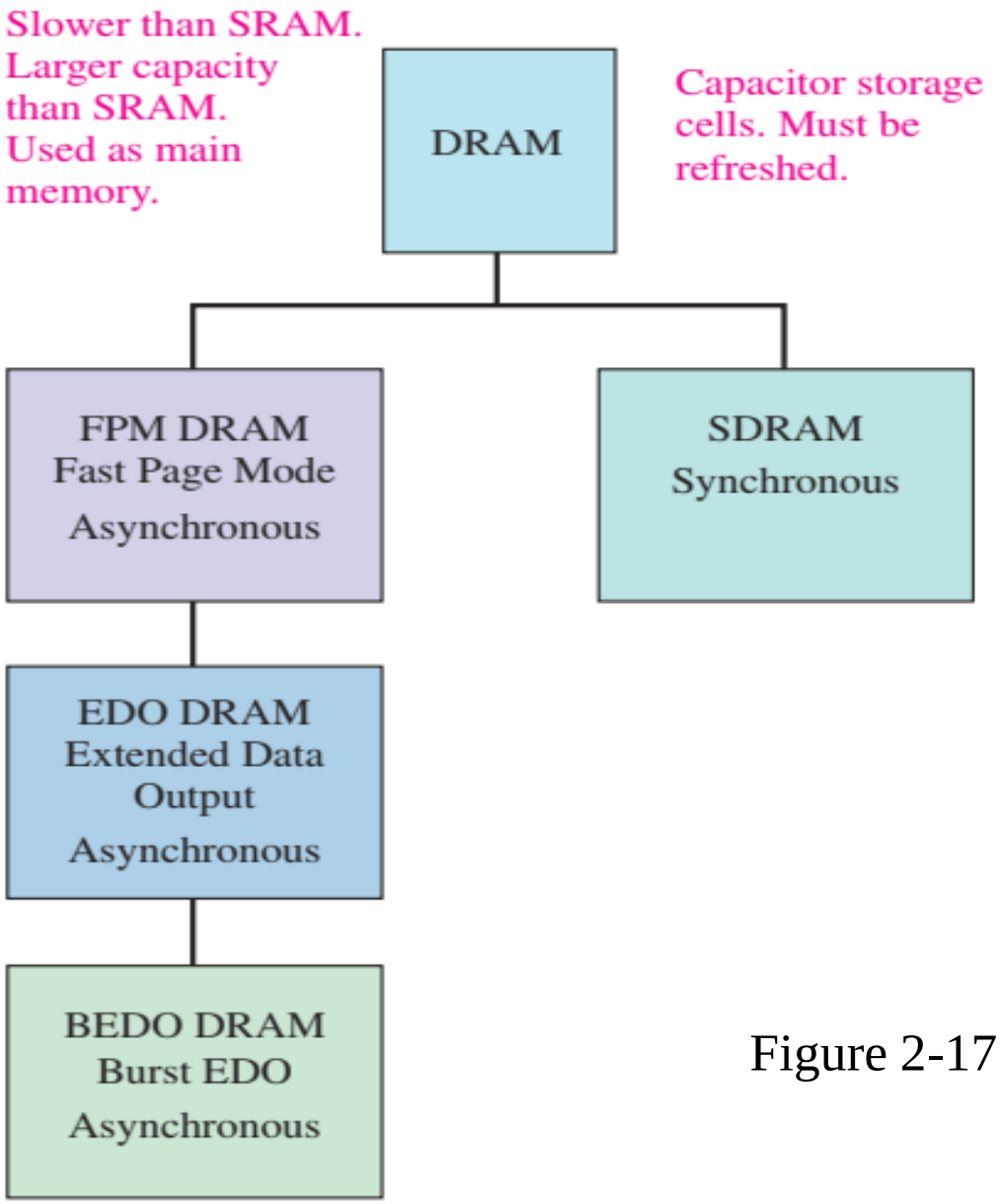


Figure 2-17

ROMs: Figure 2-18 shows the ROM types.

ROM is used in a computer to store the BIOS (Basic Input/Output System). These are programs that are used to perform fundamental supervisory and support functions for the computer. For example, BIOS programs stored in the ROM control certain video monitor functions, provide for disk formatting, scan the keyboard for inputs, and control certain printer functions.

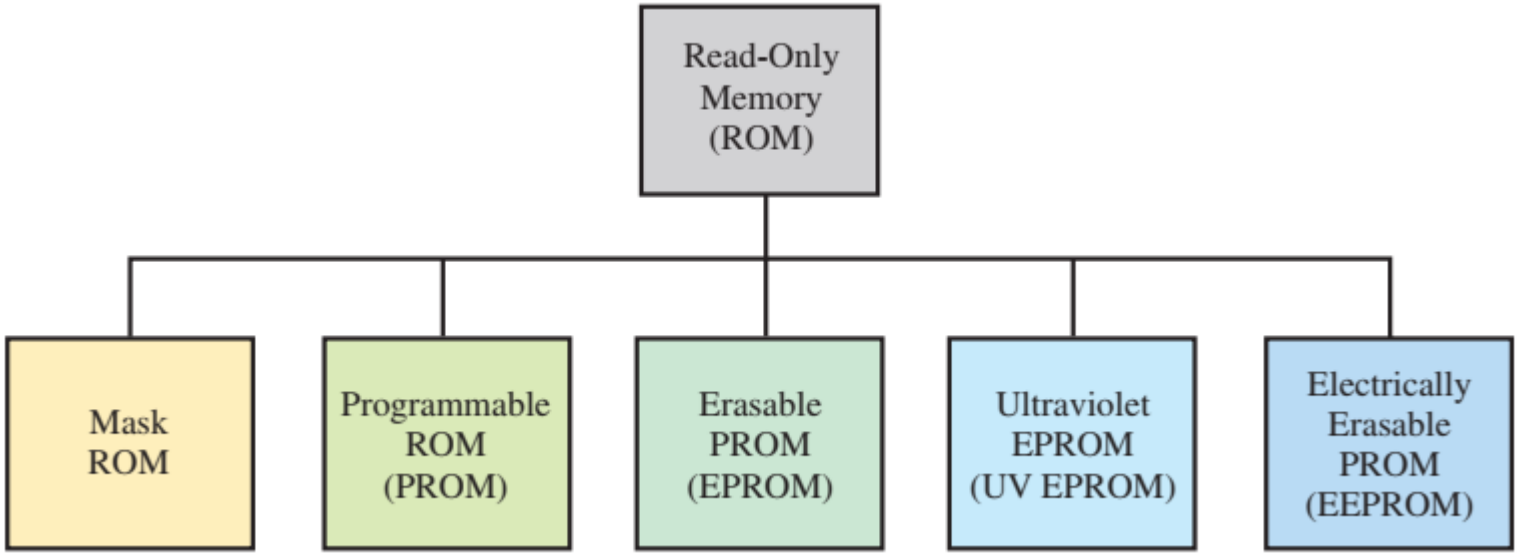


Figure 2-18

- **Flash memories** are high-density read/write memories that are nonvolatile, which means that data can be stored indefinitely without power.
- A 0 is stored when there is more charge and a 1 is stored when there is less or no charge.
- There are three major operations in a flash memory: **programming, read** and **erase**.

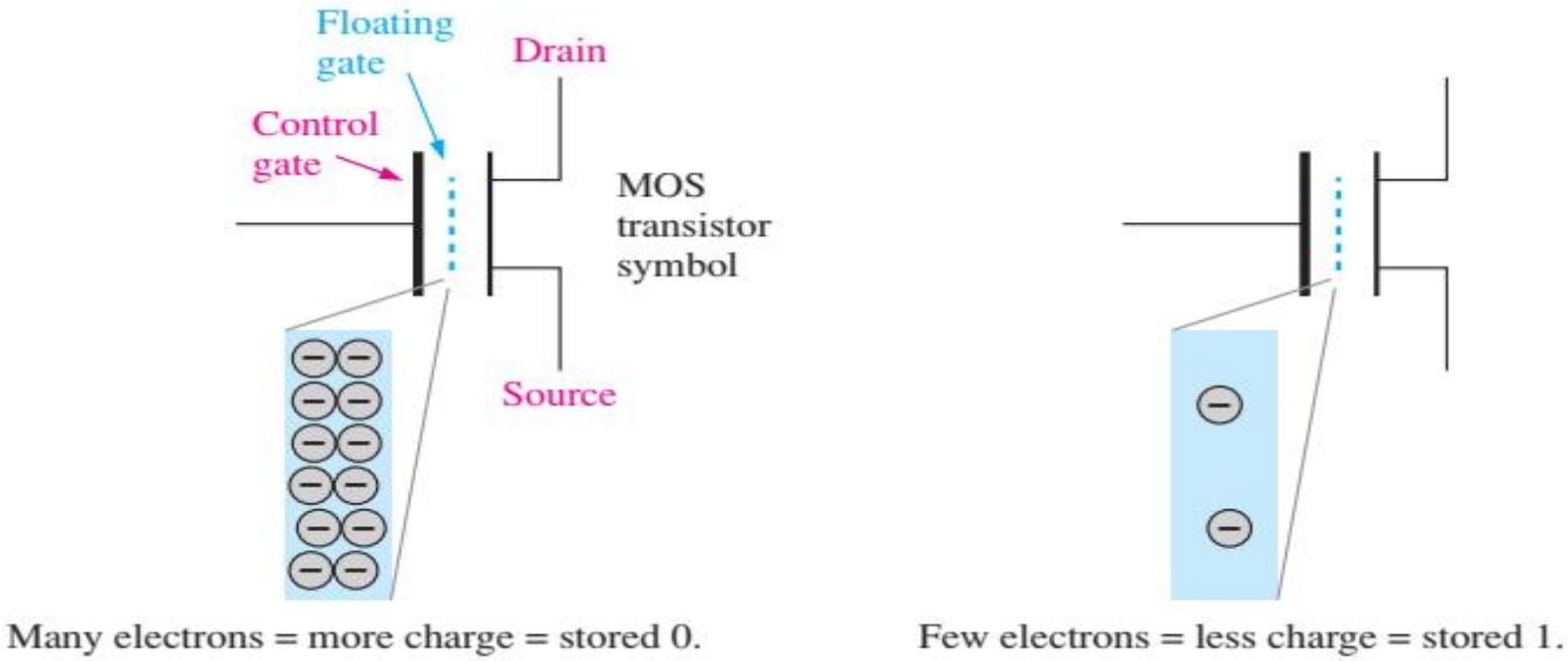


Figure 2-19 The storage cell in the flash memory.

- **Programming:** Initially, all cells are at the 1 state because charge was removed from each cell in a previous erase operation.
- The programming operation adds electrons (charge) to the floating gate of those cells that are to store a 0. No charge is added to store a 1.
- Application of a sufficient positive voltage to the control gate with respect to the source during programming attracts electrons to the floating gate as shown in Fig. 2-20.
- Once programmed, a cell can retain the charge for up to 100 years without any external power.

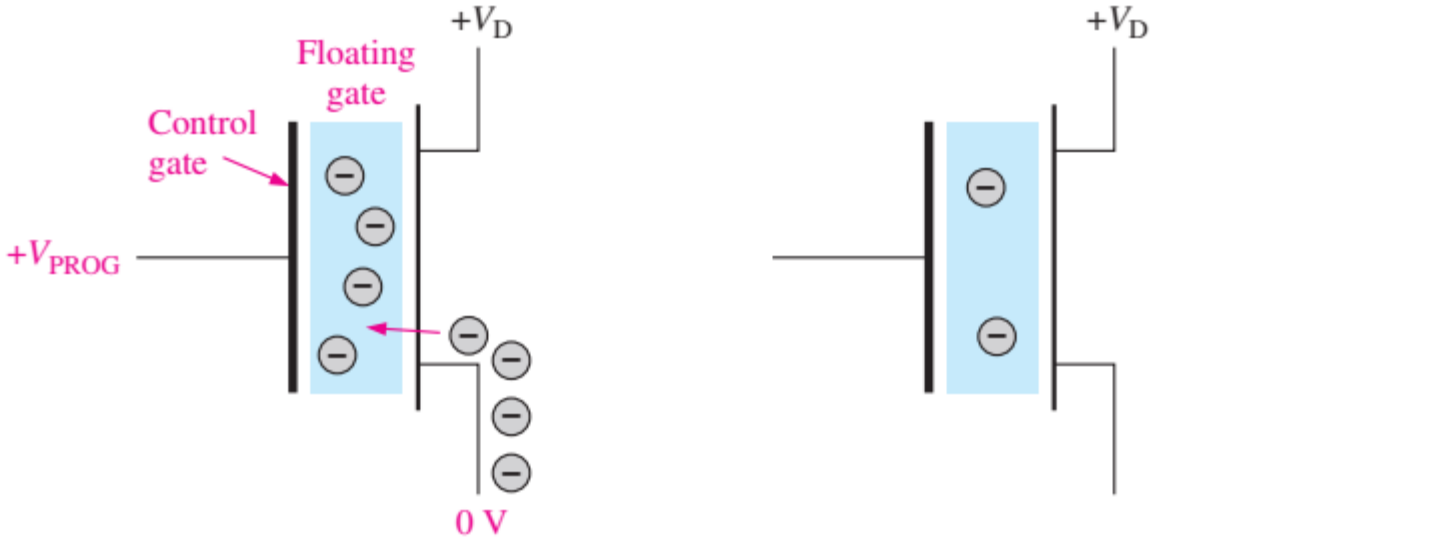
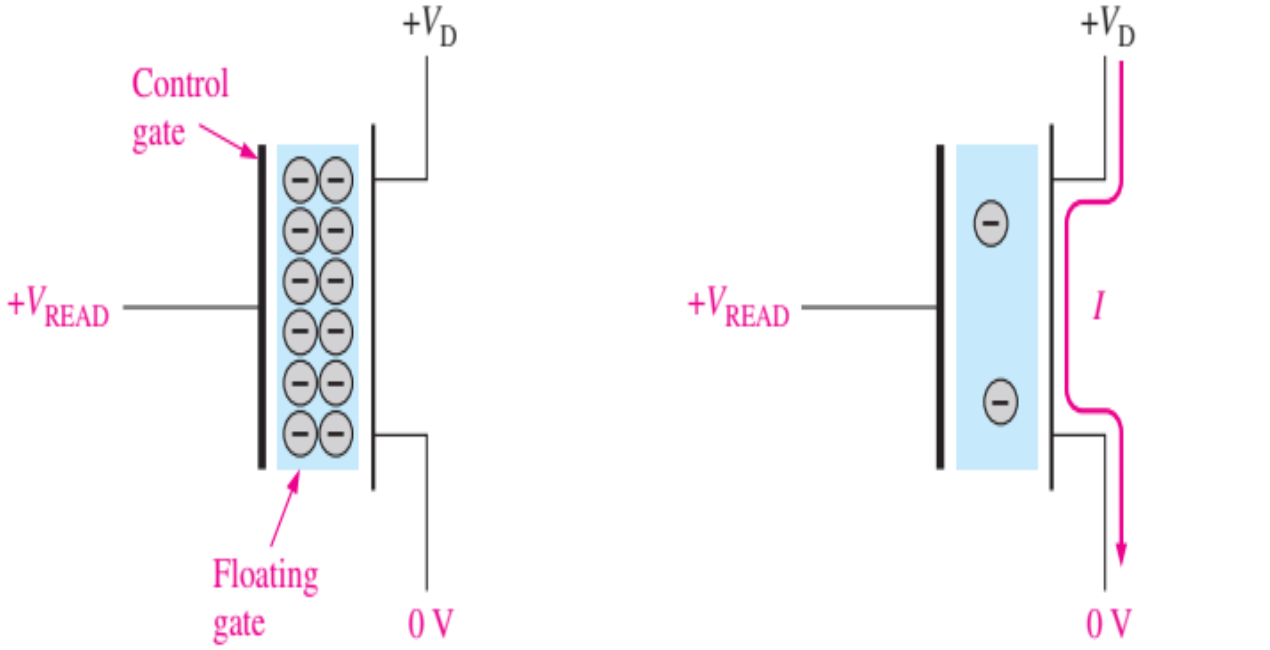


Fig. 2-20

To store a 0, a sufficient positive voltage is applied to the control gate with respect to the source to add charge to the floating gate during programming.

To store a 1, no charge is added and the cell is left in the erased condition.

- **Read:** A positive voltage is applied to the control gate. The amount of charge present on the floating gate determines whether or not the voltage applied to the control gate will turn on the transistor, as shown in Fig. 2-21.

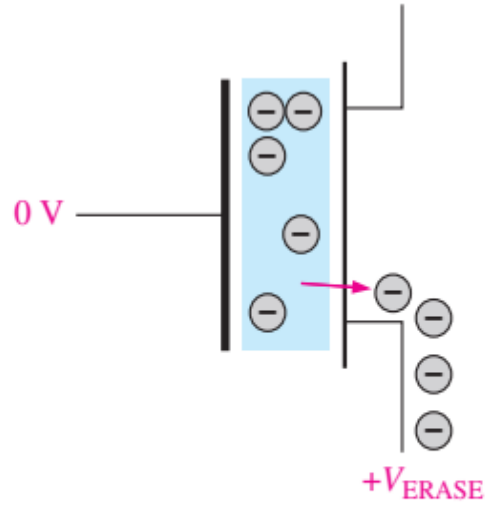


When a 0 is read, the transistor remains off because the charge on the floating gate prevents the read voltage from exceeding the turn-on threshold.

When a 1 is read, the transistor turns on because the absence of charge on the floating gate allows the read voltage to exceed the turn-on threshold.

Fig. 2-21 The read operation.

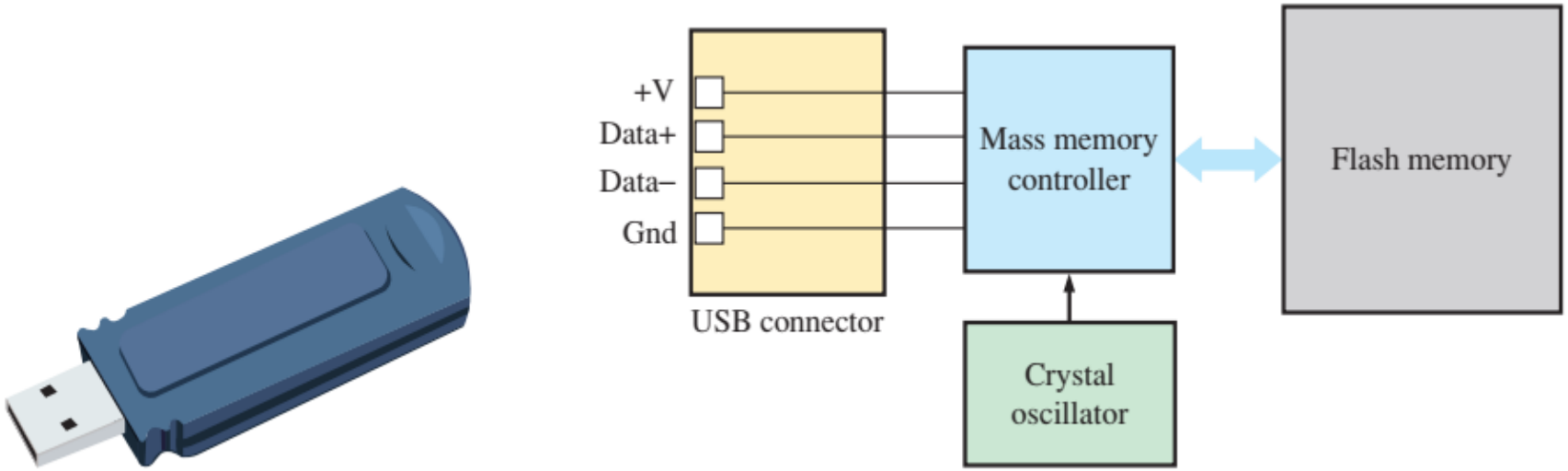
- **Erase:** During an erase operation, charge is removed from all the memory cells. It is opposite in polarity to that used in programming. This voltage attracts electrons from the floating gate and depletes it of charge, as shown in Fig. 2-22.
- A flash memory is always erased prior to being programmed.



To erase a cell, a sufficient positive voltage is applied to the source with respect to the control gate to remove charge from the floating gate during the erase operation.

Fig. 2-22 The erase operation.

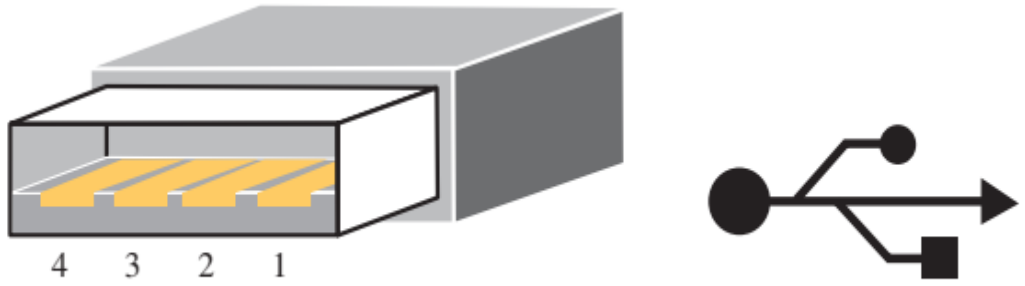
- **USB Flash Drive:** A USB flash drive consists of a flash memory connected to a standard USB connector housed in a small case.
- The USB connector can be plugged into a port on a PC and obtains power from the computer.
- A typical flash drive is shown in Fig. 2-23. Figure 2-24 shows the type-A USB connector and the USB icon.



(a) Typical USB flash drive

(b) Basic block diagram

Fig. 2-23.



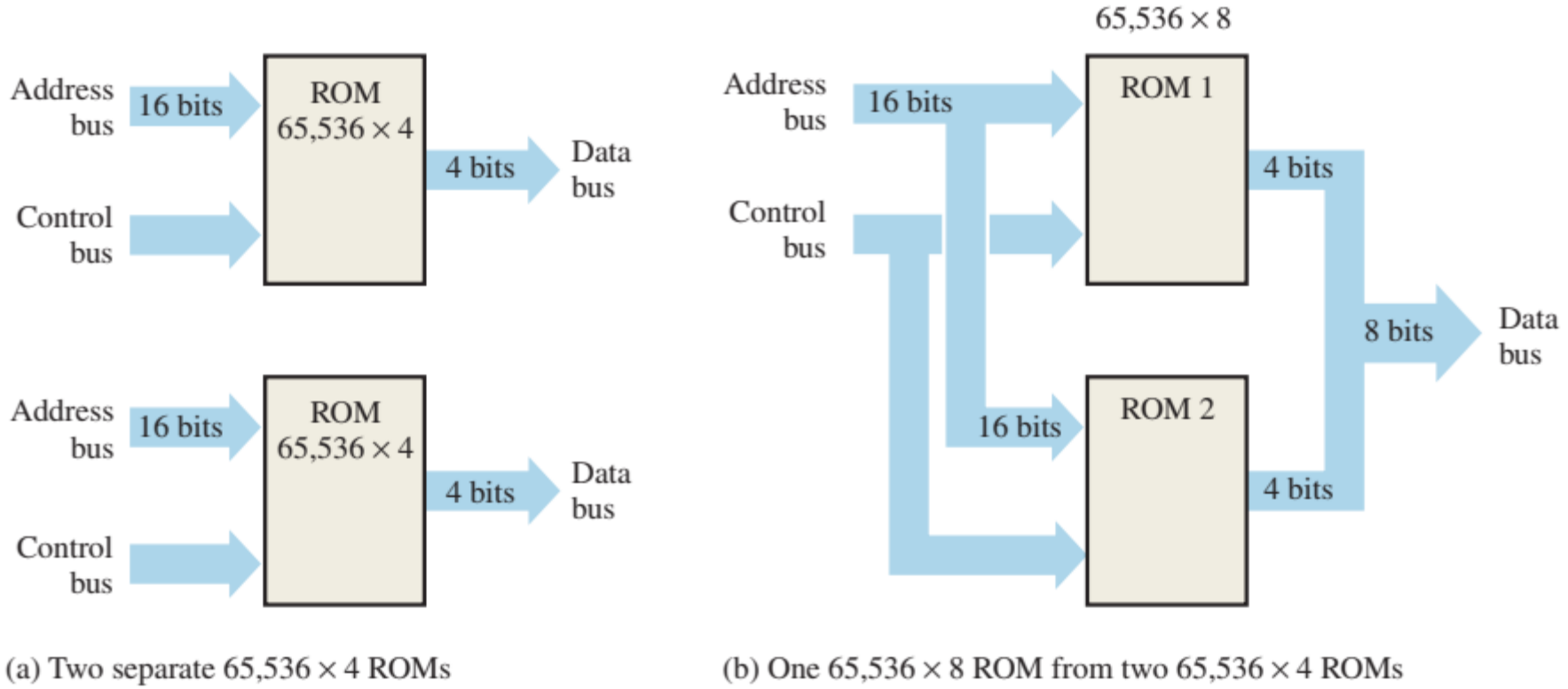
(a) Type A USB connector

(b) USB icon

Fig. 2-24.

Memory Expansion

- **Word-Length Expansion:** The number of bits in the data bus must be increased.
- Figure 2-25 shows the expansion of two 65,536 x 4 ROMs into a 65,536 x 8 ROM.

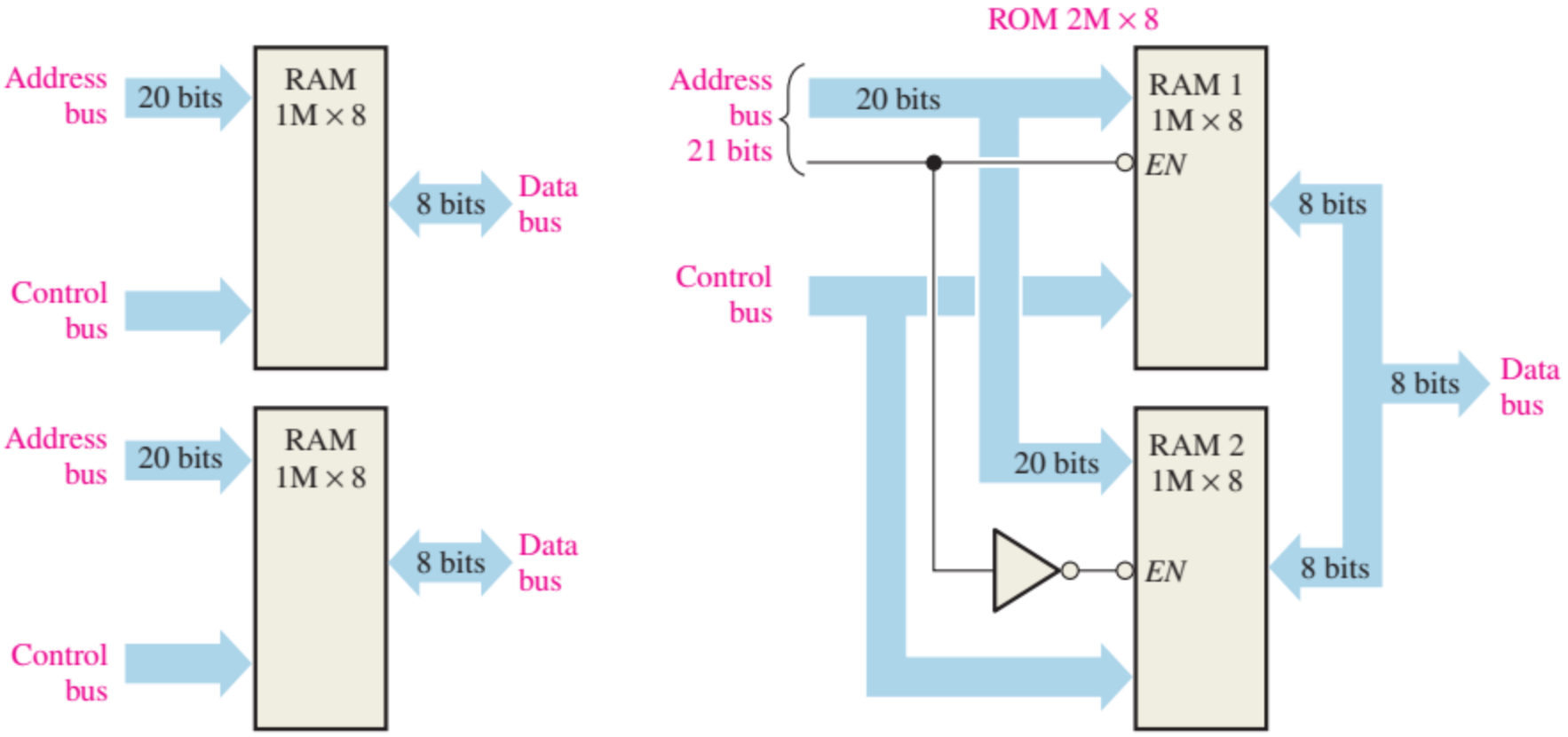


(a) Two separate 65,536 × 4 ROMs

(b) One 65,536 × 8 ROM from two 65,536 × 4 ROMs

Fig. 2-25.

- **Word-Capacity Expansion:** The number of address bits must be increased.
- Figure 2-26 shows two 1M x 8 RAMs are expanded to form a 2M x 8 RAMs.



(a) Individual memories each store 1,048,576 8-bit words

(b) Memories expanded to form a 2M × 8 RAM requiring a 21-bit address bus

Fig. 2-26.

- **Architecture of CMOS SRAM:** Figure 2-27 shows a typical SRAM cell in CMOS technology.
- The circuit consists of two cross-coupled inverters and two access transistors, Q5 and Q6.
- The access transistors are turned on when the word line is selected and its voltage raised to V_{DD}, and they connect the flip-flop to the column line (bit line).
- This circuit is known as six-transistor or 6T cell.

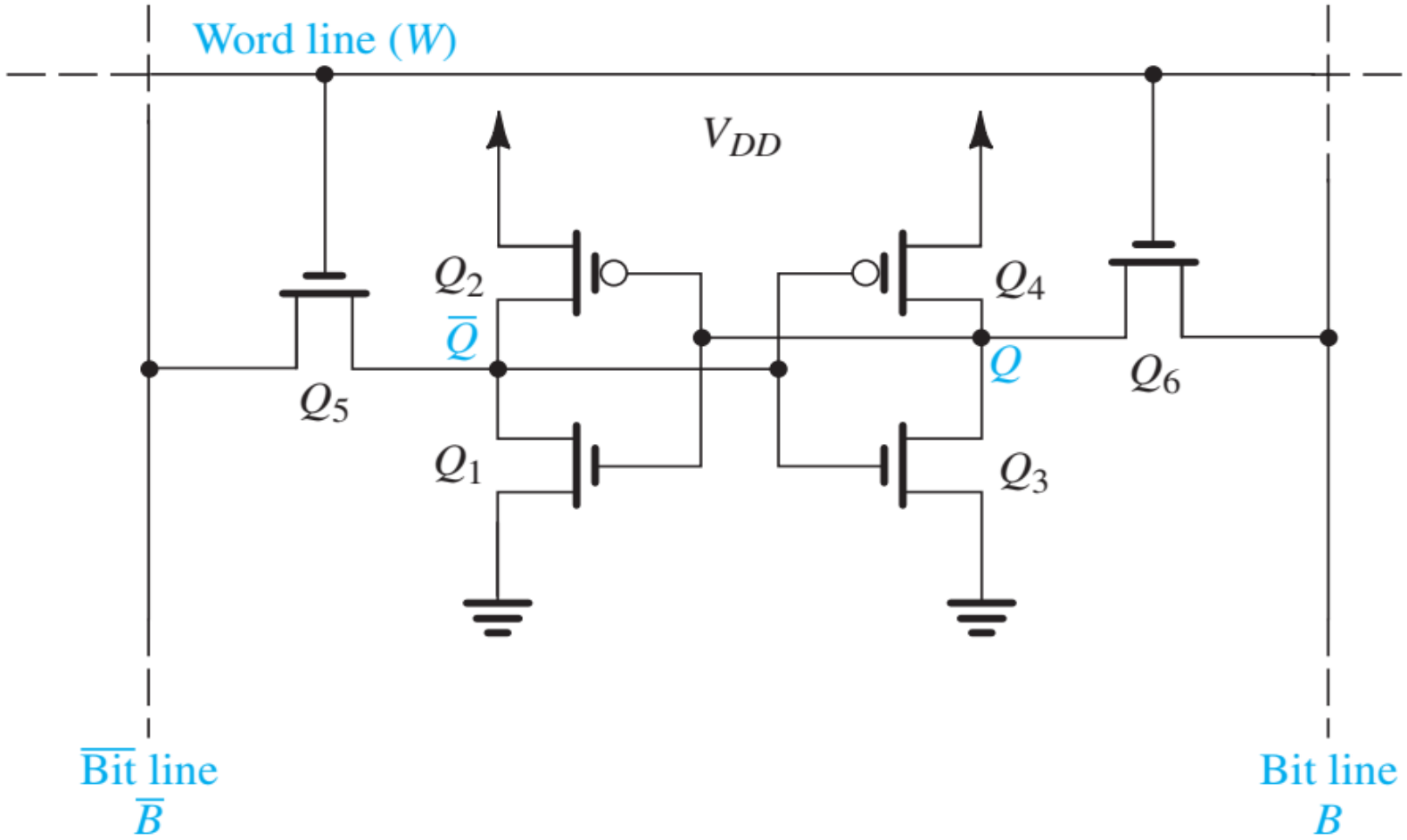


Fig. 2-27.