CHAPTER 15

REDUCTION OF STATE TABLES STATE ASSIGNMENT

Contents

Objectives

1. Define equivalent states, state several ways of testing for state equivalence, and determine if two states are equivalent.
2. Define equivalent sequential circuits and determine if two circuits are equivalent.
3. Reduce a state table to a minimum number of rows.
4. Specify a suitable set of state assignments for a state table, eliminating those assignments which are equivalent with respect to the cost of realizing the circuit
5. State three guidelines which are useful in making state assignments, and apply these to making a good state assignment for a given state table
6. Given a state table and assignment, form the transition table and derive flip-flop input equations
7. Make a one-hot state assignment for a state graph and write the next state and output equations by inspection.

15.1 Elimination of Redundant States

Table 15-1. State Table for Sequence Detector

Input Sequence	Present State	Next State X=0	Next State X=1	Present Output X=0	Present Output X=1
reset	A	B	C	0	0
0	B	D	E	0	0
1	C	F	G	0	0
00	D	H	I	0	0
01	E	J	K	0	0
10	F	L	M	0	0
11	G	N	P	0	0
000	H	A	A	0	0
001	I	A	A	0	0
010	J	A	A	0	1
011	K	A	A	0	0
100	L	A	A	0	1
101	M	A	A	0	0
110	N	A	A	0	0
111	P	A	A	0	0

15.1 Elimination of Redundant States

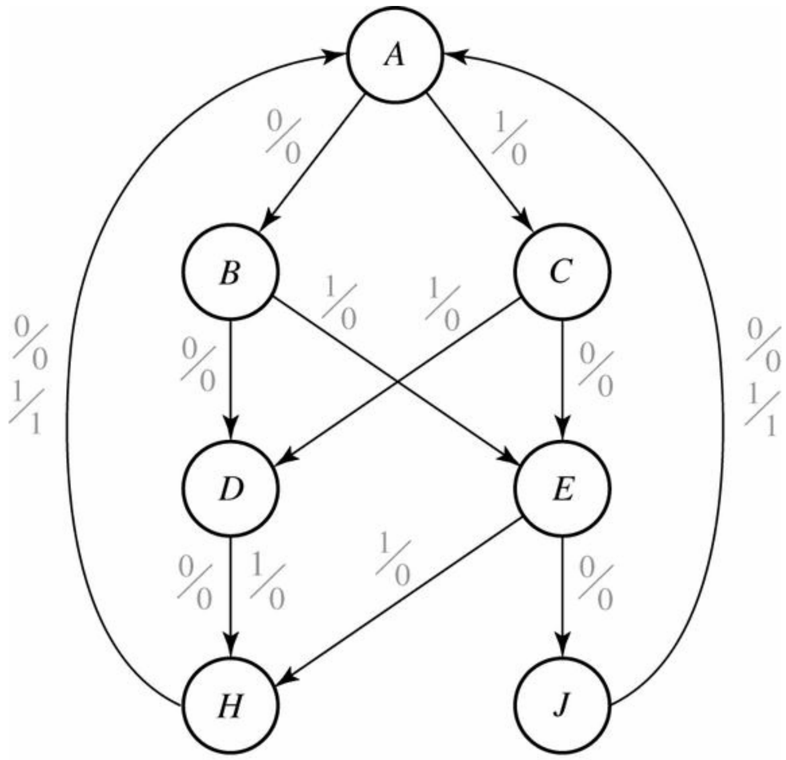
Table 15-2. State Table for Sequence Detector

Present State	Next State		Present Output	
	X=0	X=1	X=0	X=1
A	B	C	0	0
B	D	E	0	0
C	~~F~~ E	~~G~~ D	0	0
D	H	~~I~~ H	0	0
E	J	~~K~~ H	0	0
~~F~~	~~L~~ ~~J~~	~~M~~ ~~H~~	~~0~~	~~0~~
~~G~~	~~N~~ ~~H~~	~~P~~ ~~H~~	~~0~~	~~0~~
H	A	A	0	0
~~I~~	~~A~~	~~A~~	~~0~~	~~0~~
J	A	A	0	1
~~K~~	~~A~~	~~A~~	~~0~~	~~0~~
~~L~~	~~A~~	~~A~~	~~0~~	~~1~~
~~M~~	~~A~~	~~A~~	~~0~~	~~0~~
~~N~~	~~A~~	~~A~~	~~0~~	~~0~~
~~P~~	~~A~~	~~A~~	~~0~~	~~0~~

15.1 Elimination of Redundant States

Fig 15-1. Reduced State Table and Graph for Sequence Detector

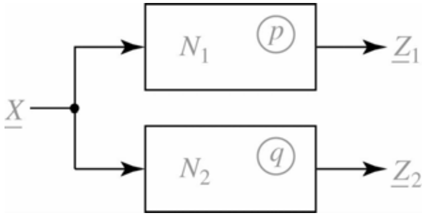
Present State	Next State X=0	Next State X=1	Present Output X=0	Present Output X=1
A	B	C	0	0
B	D	E	0	0
C	E	D	0	0
D	H	H	0	0
E	J	H	0	0
H	A	A	0	0
J	A	A	0	1



(b)

15.2 Equivalent States

Fig 15-2.



$\underline{Z}_1 = \lambda_1(p, \underline{X}) \qquad \underline{Z}_2 = \lambda_2(q, \underline{X})$

Definition 15.1

Let N_1 and N_2 be sequential circuits(not necessarily different). Let $\underline{X}$ represent a sequence of inputs of arbitrary length. Then state p in N_1 is equivalent to state q in N_2 iff $\lambda_1(p, \underline{X}) = \lambda_2(q, \underline{X})$ for every possible input sequence $\underline{X}$.

Theorem 15.1

Two states p and q of a sequential circuit are equivalent iff for every single input X, the outputs are the same and the next states are equivalent, that is,

$$\lambda(p, X) = \lambda(q, X) \quad \text{and} \quad \delta(p, X) = \delta(q, X)$$

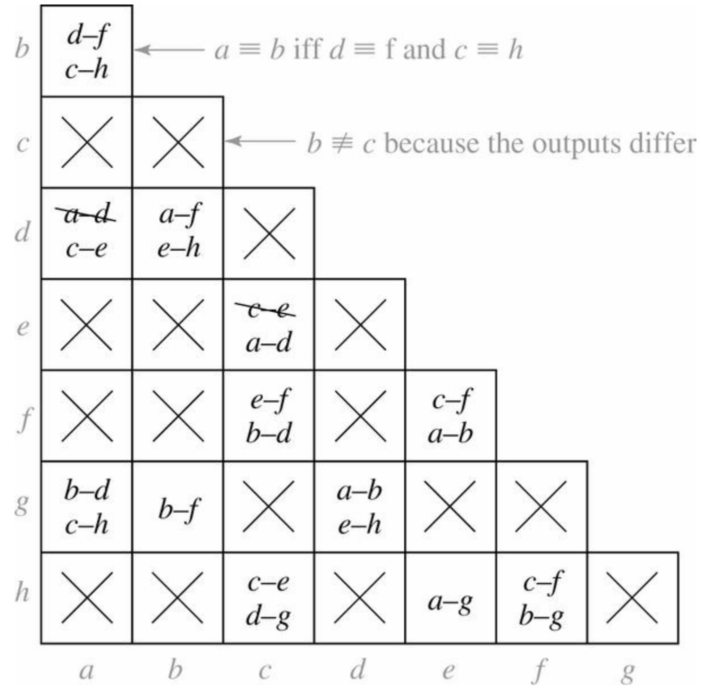
15.3 Determination of State Equivalence Using an Implication Table

Table 15-3.

Present State	Next State X=0	Next State X=1	Present Output X=0
a	d	c	0
b	f	h	0
c	e	d	1
d	a	e	0
e	c	a	1
f	f	b	1
g	b	h	0
h	c	g	1

By Theorem 15.1

Fig 15-3. Implication Chart for Table 15-3



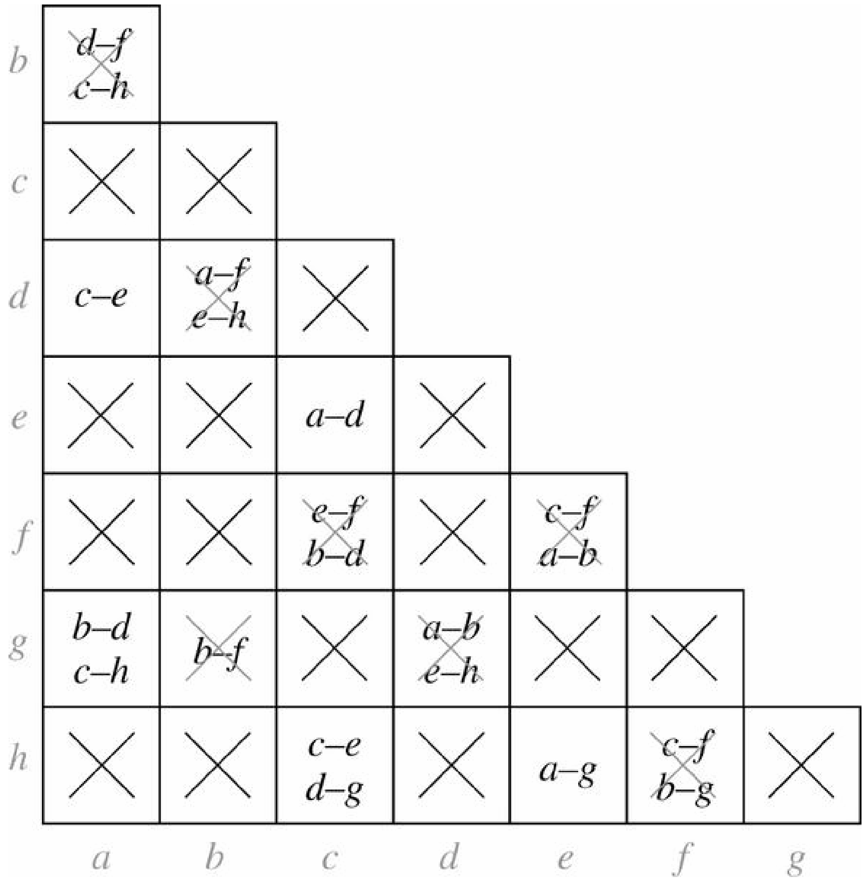
$$a \equiv b \quad \text{iff} \quad d \equiv f \quad \text{and} \quad c \equiv h$$

$$a \equiv d \quad \text{iff} \quad a \equiv d \quad \text{and} \quad c \equiv e$$

$$a \equiv g \quad \text{iff} \quad b \equiv d \quad \text{and} \quad c \equiv h$$

15.3 Implication Chart After First Pass

Fig 15-4. Implication Chart After First Pass



15.3 Implication Chart After First Pass

Fig 15-5. Implication Chart After Second Pass

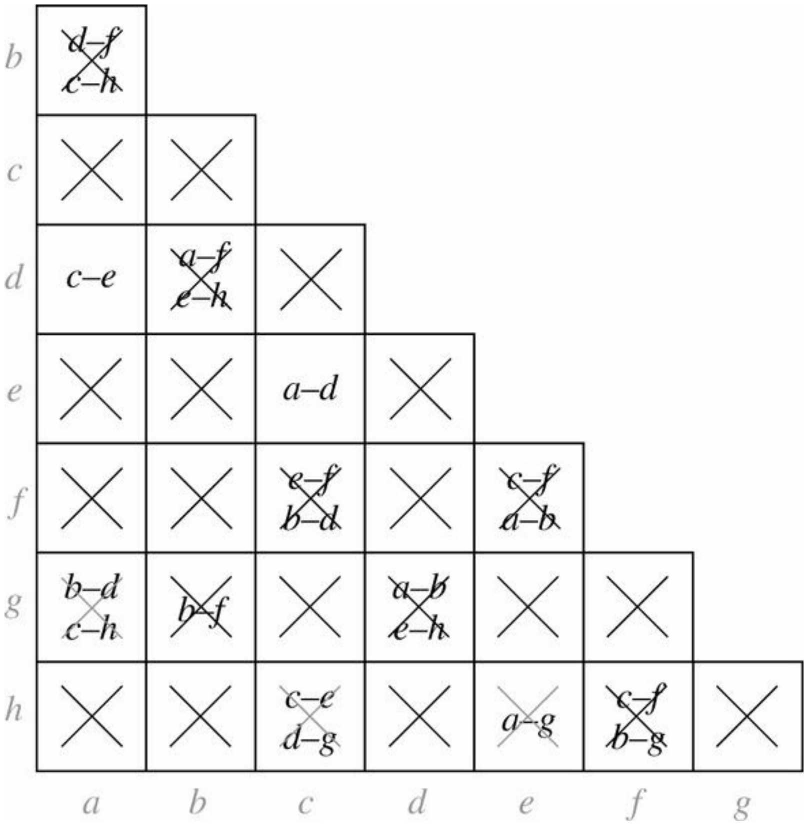


Table 15-4.

Present State	Next State X=0	Next State 1	Output
a	a	c	0
b	f	h	0
c	c	a	1
f	f	b	1
g	b	h	0
h	c	g	1

15.4 Equivalent Sequential Circuits

Definition 15.2

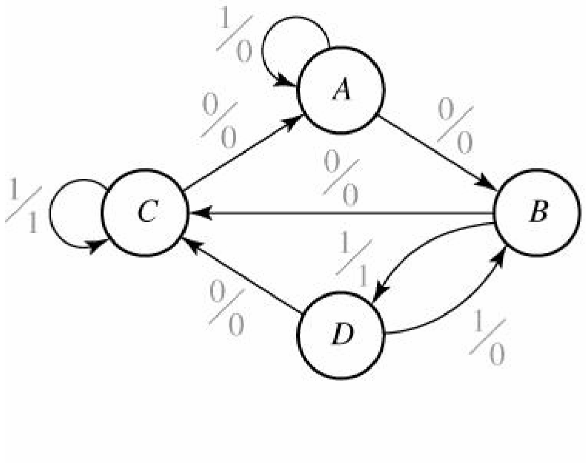
Sequential circuit N_1 is equivalent to sequential circuit N_2 if for each state p in N_1, there is a state q in N_2 such that $p \equiv q$, and conversely, for each state s in N_2, there is a state t in N_1 such that $s \equiv t$

15.4 Equivalent Sequential Circuits

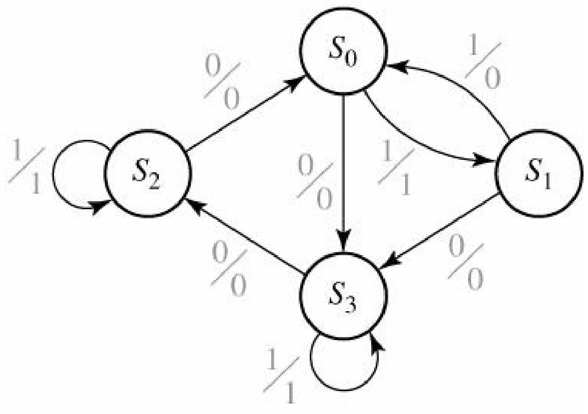
Fig 15-6. Tables and Graphs for Equivalent Circuits

	N_1			
	X=0	X=1	X=0	X=1
A	B	A	0	0
B	C	D	0	1
C	A	C	0	1
D	C	B	0	0

	N_2			
	X=0	X=1	X=0	X=1
S_0	S_3	S_1	0	1
S_1	S_3	S_0	0	0
S_2	S_0	S_2	0	0
S_3	S_2	S_3	0	1



(a)



(b)

15.4 Equivalent Sequential Circuits

Fig 15-7. Implication Tables for Determining Circuit Equivalence

	A	B	C	D
S_0	×	C–S_3 D–S_1	A–S_3 C–S_1	×
S_1	B–S_3 A–S_0	×	×	C–S_3 B–S_0
S_2	B–S_0 A–S_2	×	×	C–S_0 B–S_2
S_3	×	C–S_2 D–S_3	A–S_2 C–S_3	×

(a)

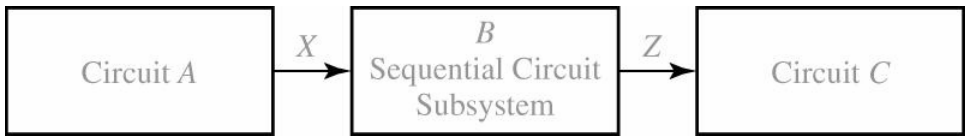
	A	B	C	D
S_0	×	C–S_3 D–S_1	~~A–S_3 C–S_1~~	×
S_1	~~B–S_3 A–S_0~~	×	×	C–S_3 B–S_0
S_2	B–S_0 A–S_2	×	×	~~C–S_0 B–S_2~~
S_3	×	~~C–S_2 D–S_3~~	A–S_2 C–S_3	×

(b)

$$A \equiv S_2 \qquad B \equiv S_0 \qquad C \equiv S_3 \qquad D \equiv S_1$$

15.5 Incompletely Specified State Tables

Fig 15-8.



The possible input-output sequence for circuit B

	t_0	t_1	t_2		t_0	t_1	t_2
X=	1	0	0	Z=	–	–	0
	1	1	0		–	–	1

(– is a don't care output)

Table 15-5. Incompletely Specified State Table

	X=0	X=1	0	1
S_0	–	S_1	–	–
S_1	S_2	S_3	–	–
S_2	S_0	–	0	–
S_3	S_0	–	1	–

	X=0	X=1	0	1
S_0	(S_0)	S_1	(0)	–
S_1	~~S_2~~ S_0	S_3	(1)	–
S_2	S_0	(S_1)	0	–
S_3	S_0	(S_3)	1	–

	X=0	X=1	0	1
S_0	S_0	S_1	0	–
S_1	S_0	S_1	1	–

$$S_0 \equiv S_2, S_1 \equiv S_3$$

15.6 Derivation of Flip-Flop Input Equations

The procedure to drive the flip-flop input equations:

1. Assign flip-flop state values to correspond to the states in the reduced table
2. Construct a transition table which gives the next states of the flip-flops as a function of the present states and inputs
3. Derive the next-state maps from the transition table
4. Find flip-flop input maps from the next-state maps using the techniques developed in Unit 12 and find the flip-flop input equations from maps

15.6 Derivation of Flip-Flop Input Equations

Table 15-6

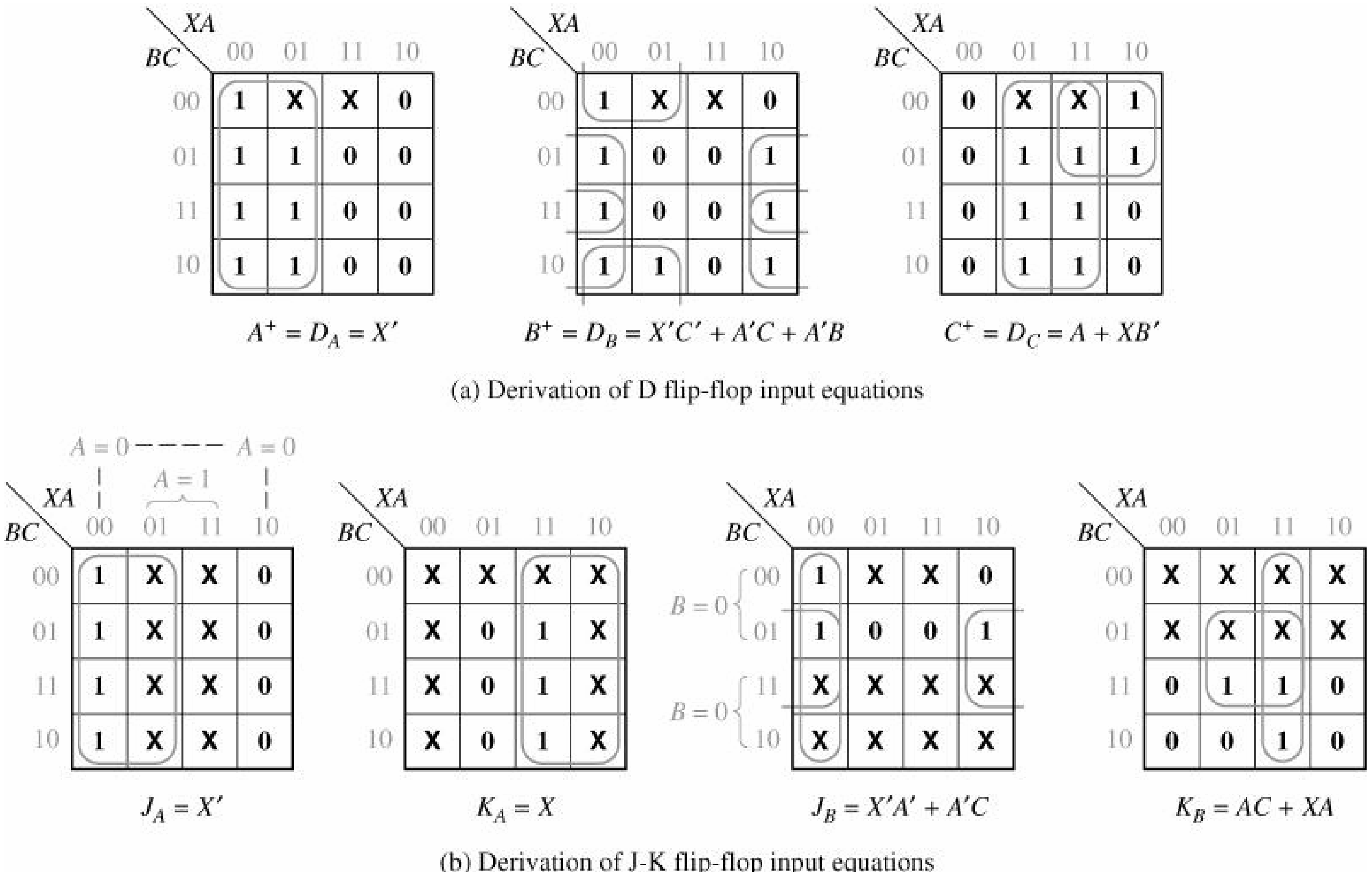
	X=0	X=1	0	1
S_0	S_1	S_2	0	0
S_1	S_3	S_2	0	0
S_2	S_1	S_4	0	0
S_3	S_5	S_2	0	0
S_4	S_1	S_6	0	0
S_5	S_5	S_2	1	0
S_6	S_1	S_6	0	1

	$A^+B^+C^+$		Z	
ABC	X=0	X=1	0	1
000	110	001	0	0
110	111	001	0	0
001	110	011	0	0
111	101	001	0	0
011	110	010	0	0
101	101	001	1	0
010	110	010	0	1

$$S_0 = 000,\ S_1 = 110,\ S_2 = 001,\ S_3 = 111,\ S_4 = 011,\ S_5 = 101,\ S_6 = 010$$

15.6 Derivation of Flip-Flop Input Equations

Fig. 15-9 Next-State Maps for Table 15-6



15.6 Derivation of Flip-Flop Input Equations

Table 15-7

PS	Next State X_1X_2=				Output(Z_1Z_2) X_1X_2=			
	00	01	11	10	00	01	11	10
S_0	S_0	S_0	S_1	S_1	00	00	01	01
S_1	S_1	S_3	S_2	S_1	00	10	10	00
S_2	S_3	S_3	S_2	S_2	11	11	00	00
S_3	S_0	S_3	S_2	S_0	00	00	00	00

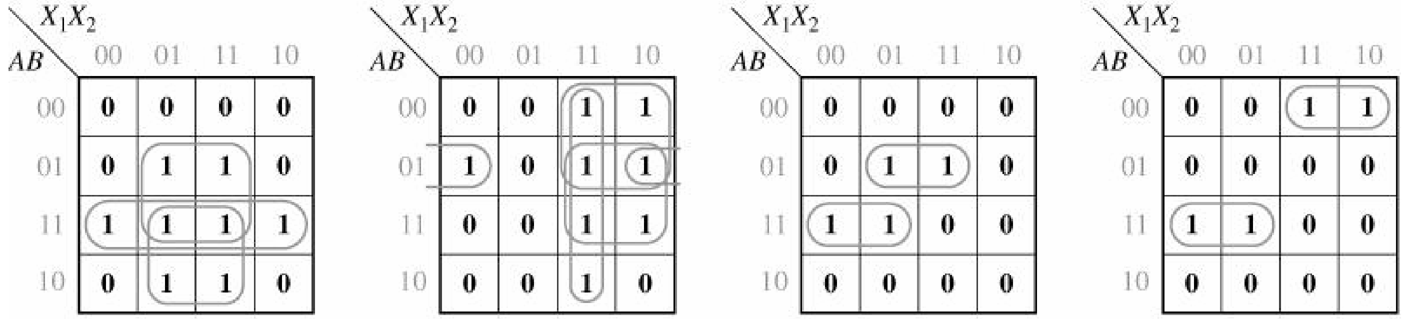
(a) State table

AB	A^+B^+ X_1X_2=				Output(Z_1Z_2) X_1X_2=			
	00	01	11	10	00	01	11	10
00	00	00	01	01	00	00	01	01
01	01	10	11	01	00	10	10	00
11	10	10	11	11	11	11	00	00
10	00	10	11	00	00	00	00	00

(b) Transition table

15.6 Derivation of Flip-Flop Input Equations

Fig.15-10 Next-State Maps for Table 15-7



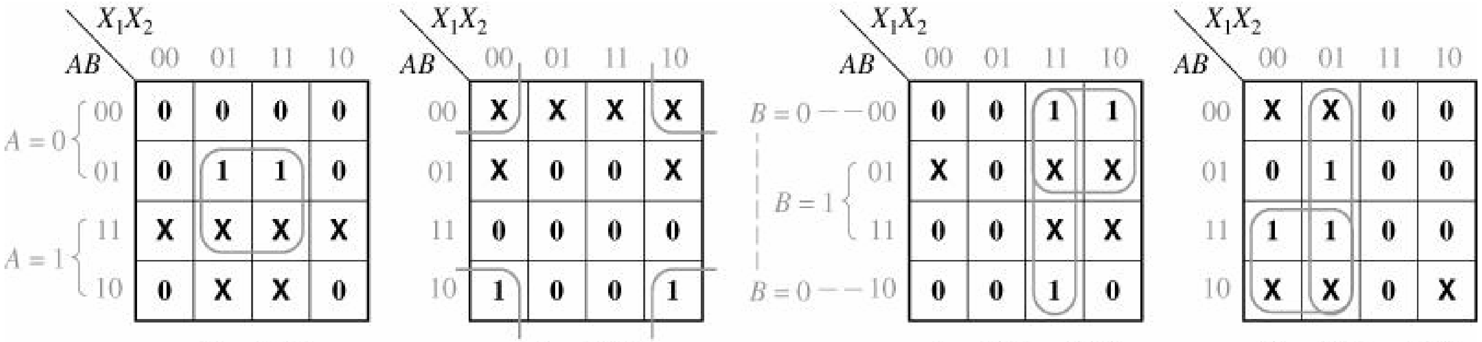
$D_A = A^+ = X_2B + AB + X_2A$

$D_B = B^+ = X_1A' + X_2A'B + X_1B + X_1X_2$

$Z_1 = X_2A'B + X_1'AB$

$Z_2 = X_1A'B' + X_1'AB$

Fig.15-11 Derivation of S-R Equations for Table 15-7



$S_A = X_2B$

$R_A = X_2'B'$

$S_B = X_1X_2 + X_1A'$

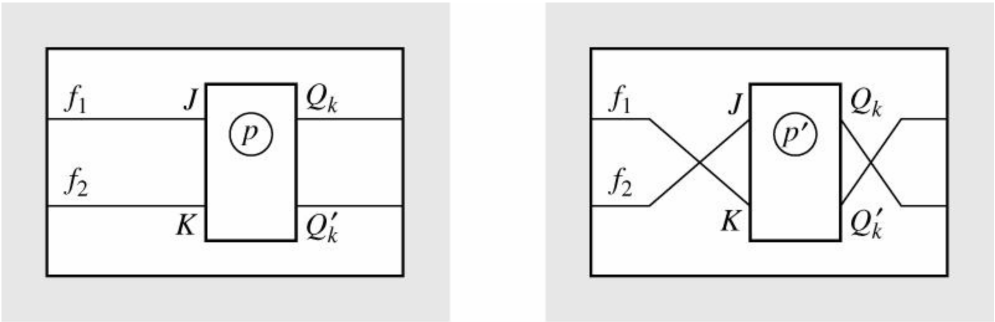
$R_B = X_1'X_2 + X_1'A$

15.7 Equivalent State Assignments

Table 15-8. State Assignments for 3-Row Tables

	1	2	3	4	5	6	7		19	20	21	22	23	24
S_0	00	00	00	00	00	00	01	…	11	11	11	11	11	11
S_1	01	01	10	10	11	11	00		00	00	01	01	10	10
S_2	10	11	01	11	01	10	10		01	10	00	10	00	01

Fig. 15-12 Equivalent Circuits Obtained by Complementing Q_k

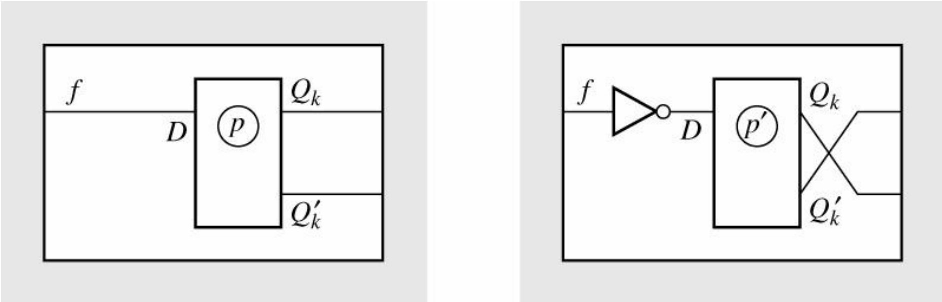


(a) Circuit *A*

(b) Circuit *B*
(identical to *A* except leads to flip-flop Q_k are crossed)

15.7 Equivalent State Assignments

Fig. 15-13 Equivalent Circuits Obtained by Complementing Q_k



(a) Circuit *A*

(b) Circuit *B* (identical to *A* except for connections to flip-flop Q_k)

Table 15-9

Assignments			Present State	Next State		Output	
A_3	B_3	C_3		X=0	1	0	1
00	00	11	S_1	S_1	S_3	0	0
01	10	10	S_2	S_2	S_1	0	1
10	01	01	S_3	S_2	S_3	1	0

15.7 Equivalent State Assignments

The resulting J and K input equations

Assignment A	Assignment B	Assignment C
$J_1 = XQ_2'$	$J_2 = XQ_1'$	$K_1 = XQ_2$
$K_1 = X'$	$K_2 = X'$	$J_1 = X'$
$J_2 = X'Q_1$	$J_1 = X'Q_2$	$K_2 = X'Q_1'$
$K_2 = X$	$K_1 = X$	$J_2 = X$
$Z = X'Q_1 + XQ_2$	$Z = X'Q_2 + XQ_1$	$Z = X'Q_1' + XQ_2'$
$D_1 = XQ_2'$	$D_2 = XQ_1'$	$D_1 = X' + Q_2'$
$D_2 = X'(Q_1 + Q_2)$	$D_1 = X'(Q_2 + Q_1)$	$D_2 = X + Q_1Q_2$

Table 15-10 Nonequivalent Assignments for Three and Four States

	3-State Assignments			4-State Assignments		
States	1	2	3	1	2	3
a	00	00	00	00	00	00
b	01	01	11	01	01	11
c	10	11	01	10	11	01
d	–	–	–	11	10	10

15.7 Equivalent State Assignments

Table 15-11 Number of Distinct(Nonequivalent)State Assignments

Number of States	Minimum Number of State Variables	Number of Distinct Assignments
2	1	1
3	2	3
4	2	3
5	3	140
6	3	420
7	3	840
8	3	840
9	4	10,810,800
…	…	…
16	4	$\approx 5.5 \times 10^{10}$

15.8 Guidelines for State Assignment

Guidelines for state assignment

1. States which have the same next state for a given input should be given adjacent assignments
2. States which are the next states of the same state should be given adjacent assignments
3. States which have the same output for a given input should be given adjacent assignments

15.8 Guidelines for State Assignment

Fig. 15-14

ABC		X=0	1	0	1
000	S_0	S_1	S_2	0	0
110	S_1	S_3	S_2	0	0
001	S_2	S_1	S_4	0	0
111	S_3	S_5	S_2	0	0
011	S_4	S_1	S_6	0	0
101	S_5	S_5	S_2	1	0
010	S_6	S_1	S_6	0	1

(a) State table

BC \ A	0	1
00	S_0	
01	S_2	S_5
11	S_4	S_3
10	S_6	S_1

BC \ A	0	1
00	S_0	
01	S_1	S_6
11	S_3	S_4
10	S_5	S_2

(b) Assignment maps

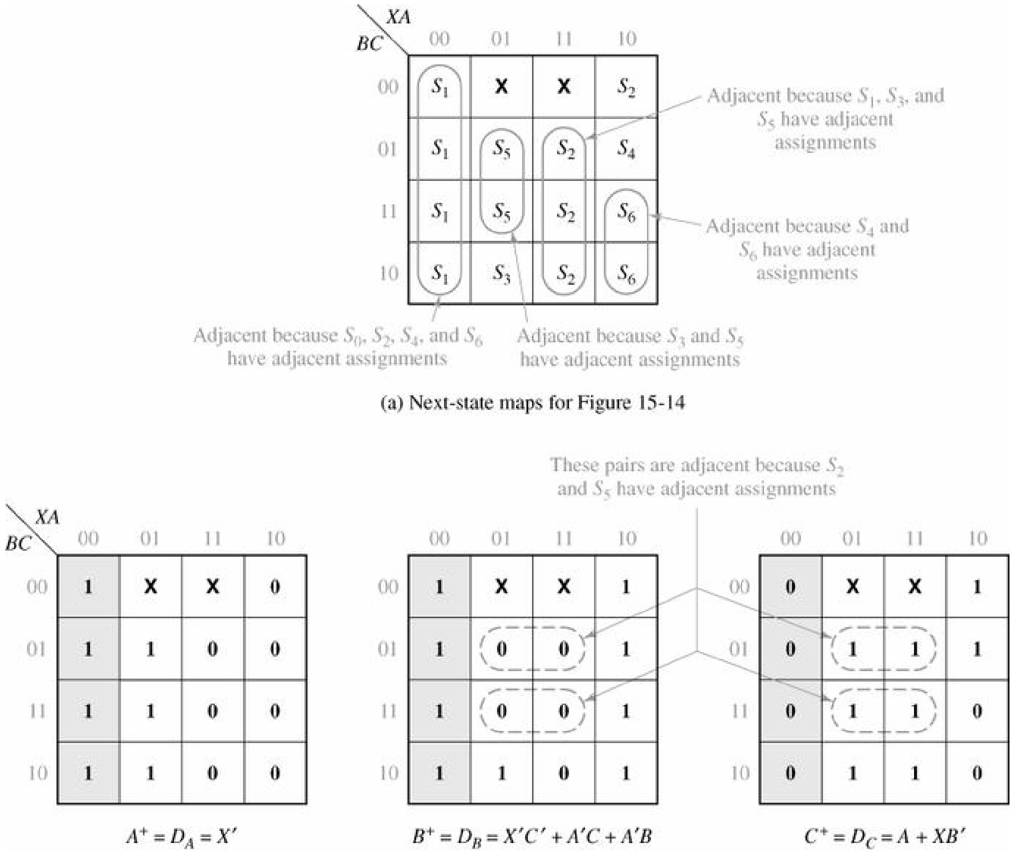
The sets of adjacent states specified by Guidelines 1 and 2

$$1.(S_0,S_1,S_3,S_5)\ \ (S_3,S_5)\ \ (S_4,S_6)\ \ (S_0,S_2,S_4,S_6)$$

$$2.(S_1,S_2)\ \ (S_2,S_3)\ \ (S_1,S_4)\ \ (S_2,S_5)2x\ \ (S_1,S_6)2x$$

15.8 Guidelines for State Assignment

Fig. 15-15 Next-State Maps for Figure 15-14



(a) Next-state maps for Figure 15-14

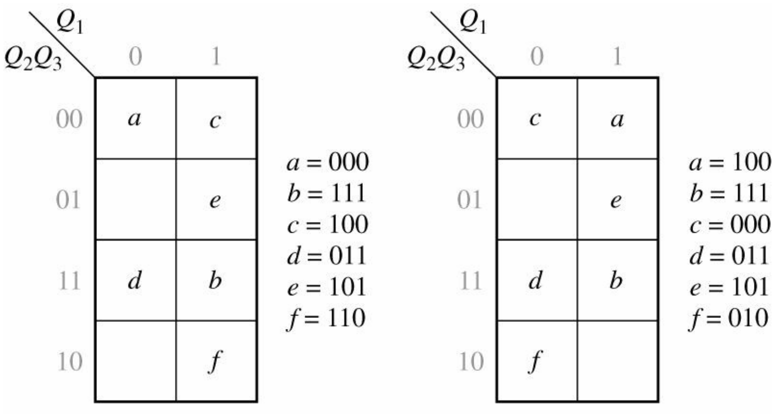
(b) Next-state maps for Figure 15-14 (cont.)

15.8 Guidelines for State Assignment

Fig. 15-16 State Table and Assignments

	X=0	1	X=0	1
a	a	c	0	0
b	d	f	0	1
c	c	a	0	0
d	d	b	0	1
e	b	f	1	0
f	c	e	1	0

(a)



(b) (c)

The sets of adjacent states specified by each Guidelines

1. $(b,d)\ \ (c,f)\ \ (b,e)$
2. $(a,c)2x\ \ (d,f)\ \ (b,d)\ \ (b,f)\ \ (c,e)$
3. $(a,c)\ \ (b,d)\ \ (e,f)$

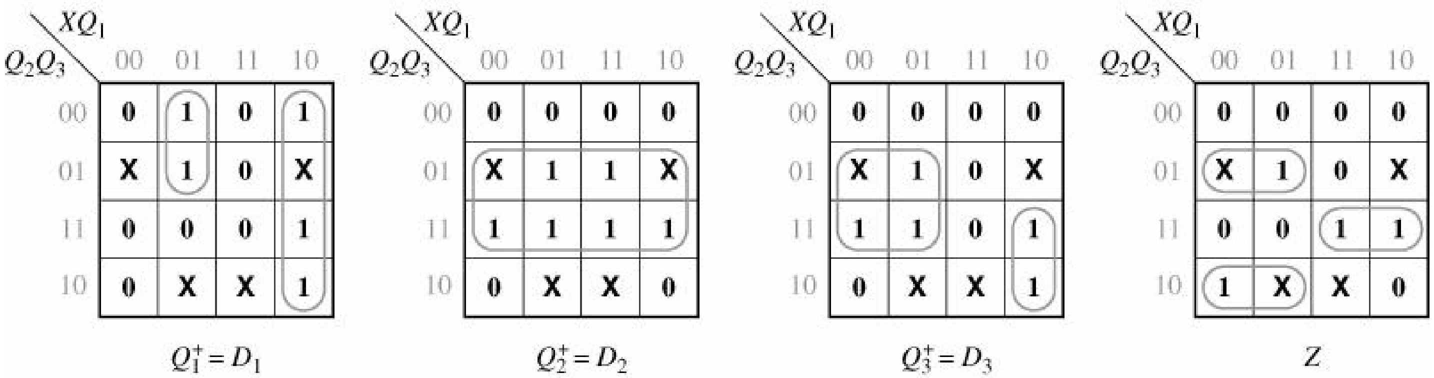
15.8 Guidelines for State Assignment

Table 15-12 Transition Table for Figure 15-16(a)

$Q_1Q_2Q_3$	$Q_1^+ Q_2^+ Q_3^+$			
	X=0	1	X=0	1
1 0 0	100	000	0	0
1 1 1	011	010	0	1
0 0 0	000	100	0	0
0 1 1	011	111	0	1
1 0 1	111	010	1	0
0 1 0	000	101	1	0

15.8 Guidelines for State Assignment

Fig. 15-17 Next-State and Output Maps for Table15-12



The D flip-flop input equations

$$D_1 = Q_1^+ = X'Q_1Q_2' + XQ_1'$$

$$D_2 = Q_2^+ = Q_3$$

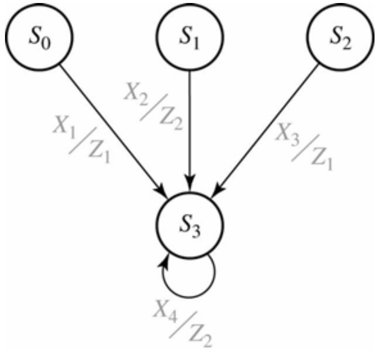
$$D_3 = Q_3^+ = XQ_1'Q_2 + X'Q_3$$

The output equations

$$Z = XQ_2Q_3 + X'Q_2'Q_3 + XQ_2Q_3'$$

15.9 Using a One-Hot State Assignment

Fig. 15-18 Partial State Graph



The One-hot assignment example

$$S_0 : Q_0Q_1Q_2Q_3 = 1000,\quad S_1 : 0100,\quad S_2 : 0010,\quad S_3 : 0001$$

The next-state equation for Q_3

$$Q_3^+ = X_1(Q_0Q_1'Q_2'Q_3') + X_2(Q_0'Q_1Q_2'Q_3') + X_3(Q_0'Q_1'Q_2Q_3') + X_4(Q_0'Q_1'Q_2'Q_3)$$

Because Q_0=1 implies Q_1= Q_2= Q_3=0,

$$Q_3^+ = X_1Q_0 + X_2Q_1 + X_3Q_2 + X_4Q_3$$

15.9 Using a One-Hot State Assignment

The One-hot assignment example by replacing Q_0 with Q'_0

$$S_0 : Q_0Q_1Q_2Q_3 = 0000,\quad S_1 : 1100,\quad S_2 : 1010,\quad S_3 : 1001$$

The modified equations

$$Q_3^+ = X_1Q_0' + X_2Q_1 + X_3Q_2 + X_4Q_3$$

$$Z_1 = X_1Q_0' + X_3Q_2,\quad Z_2 = X_2Q_1 + X_4Q_3$$

The next-state equations

$$Q_0^+ = F'R'Q_0 + FQ_2 + F'RQ_1$$

$$Q_1^+ = F'R'Q_1 + FQ_0 + F'RQ_2$$

$$Q_2^+ = F'R'Q_2 + FQ_1 + F'RQ_0$$

The output equations

$$Z_1 = Q_0,\quad Z_2 = Q_1,\quad Z_3 = Q_2$$