CHAPTER 14

Derivation of State Graphs and Tables

Contents

Objectives

1. Given a problem statement for the design of a Mealy or Moore sequential circuit, find the corresponding state graph and table.

2. Explain the significance of each state in your graph or table in terms of the input sequences required to reach that state.

3. Check your state graph using appropriate input sequences.
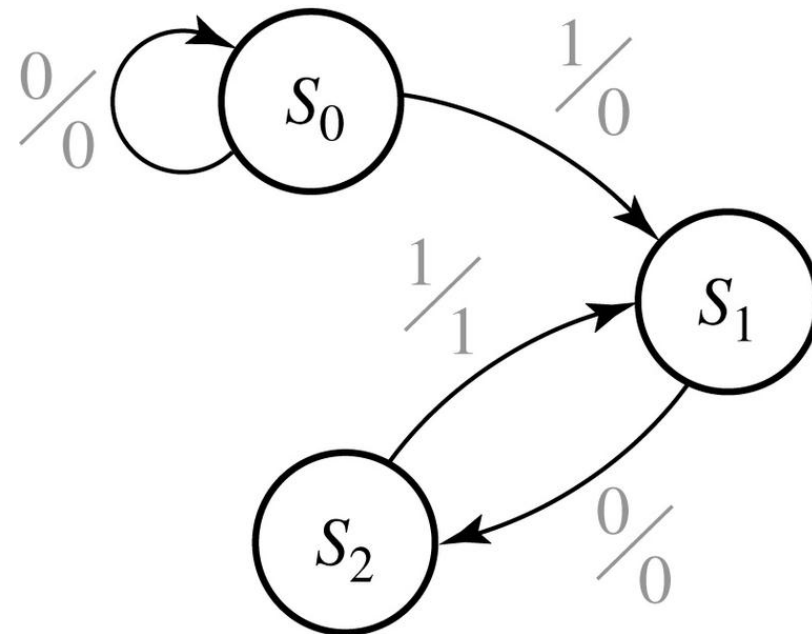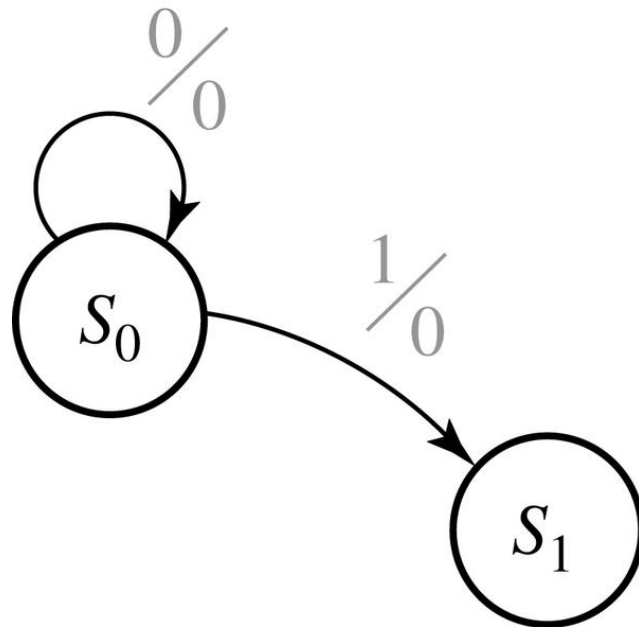
14.1 Design of a Sequence Detector

Fig 14.1 Sequence Detector to be Designed
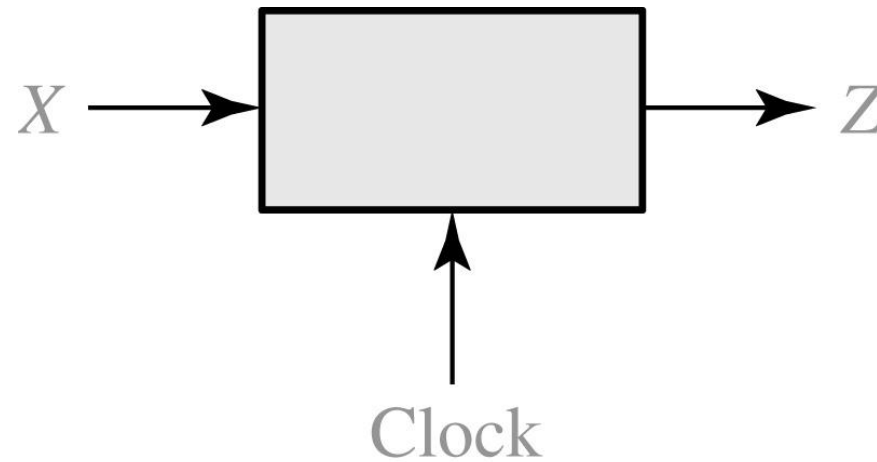
$$X = 0\ 0\ 1\ 1\ 0\ 1\ 1\ 0\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 0$$

$$Z = 0\ 0\ 0\ 0\ 0\ 1\ 0\ 0\ 0\ 0\ 0\ 1\ 0\ 1\ 0\ 0$$

(time: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15)
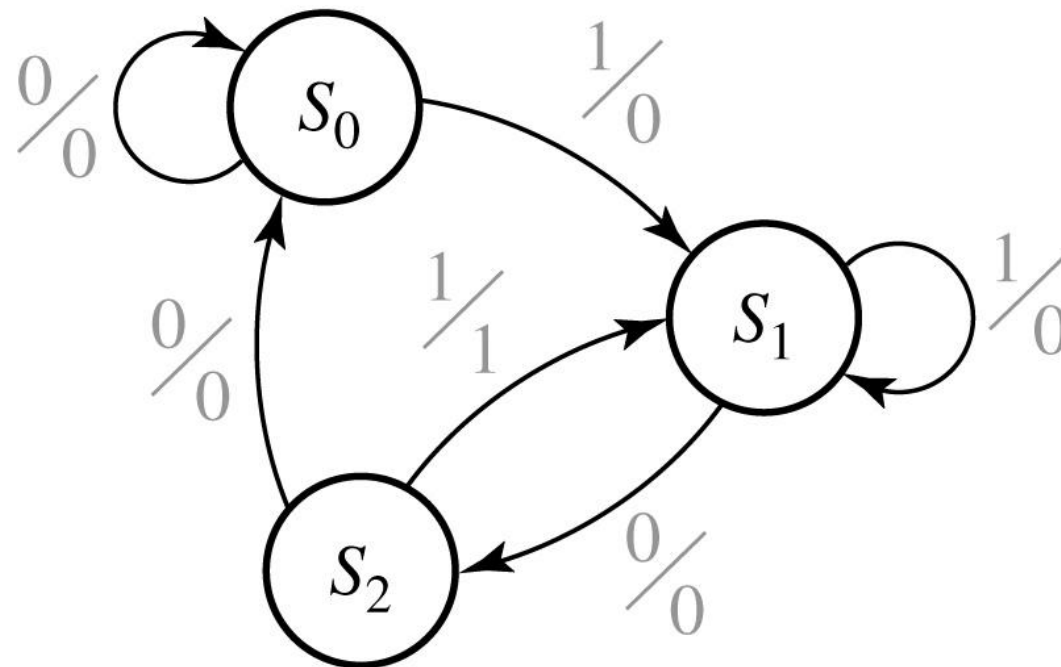
14.1 Design of a Sequence Detector

Fig 14.2 and 14.3 : Formation of State Graph

14.1 Design of a Sequence Detector

Fig 14.4 Mealy State Graph for Sequence Detector

14.1 Design of a Sequence Detector

Table 14-1, State Table

Present state	Next State		Present Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1

Table 14-2, Transition Table with State Assignment

AB	$A^+ B^+$		Z	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

14.1 Design of a Sequence Detector

Map for the output function Z (from table 1,2)

$$A^+ = X'B$$

$$B^+ = X$$

$$Z = XA$$

Fig 14.5: Final Circuit

14.1 Design of a Sequence Detector

Moore Machine Design Process
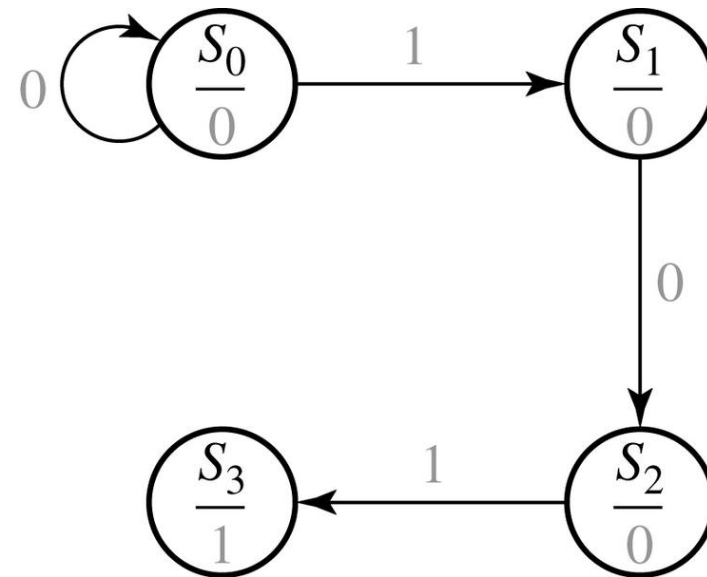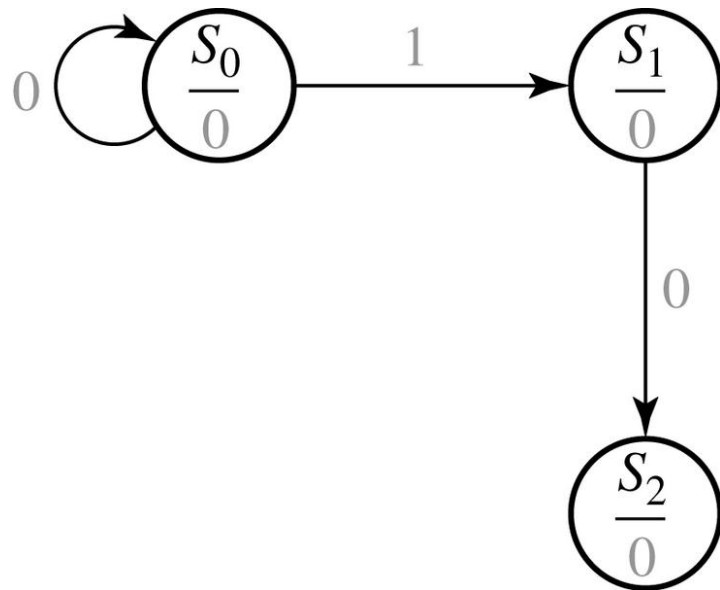
14.1 Design of a Sequence Detector

Fig 14.6 Moore State Graph for Sequence Detector

14.1 Design of a Sequence Detector

Table 14-3 State Table

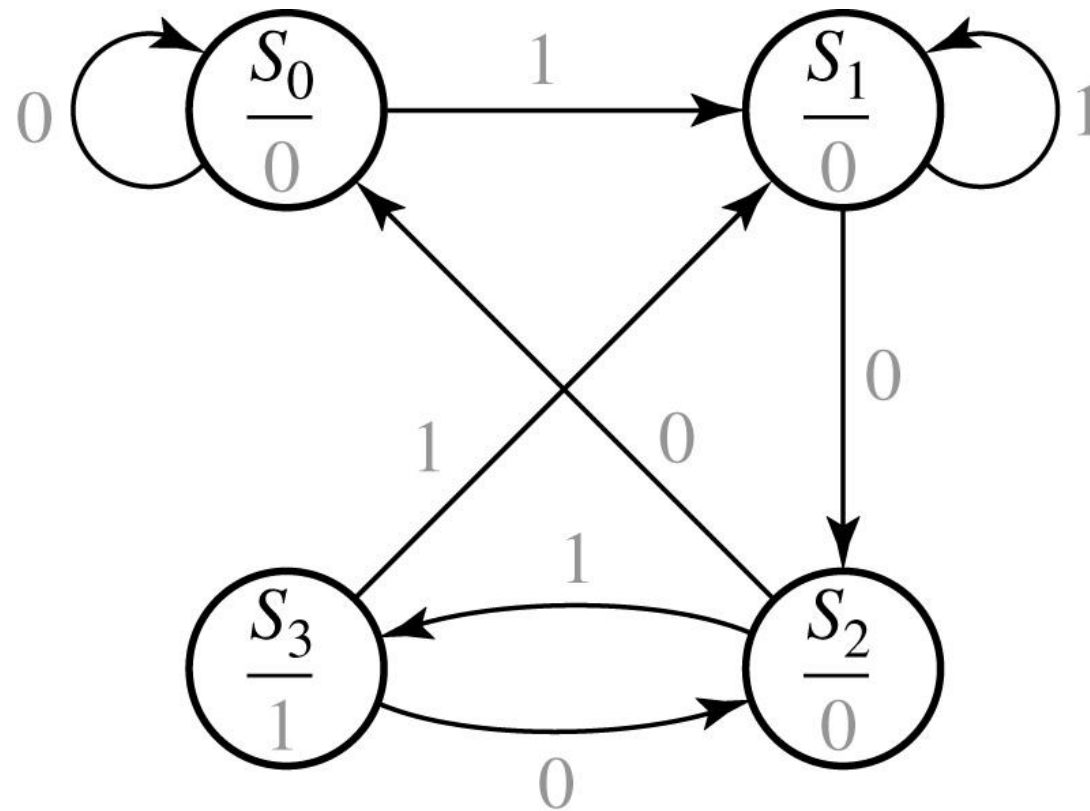Table 14-4 Transition Table
with State assignment

Present state	Next State		Present Output (Z)
	$X = 0$	$X = 1$	
S_0	S_0	S_1	0
S_1	S_2	S_1	0
S_2	S_0	S_3	0
S_3	S_2	S_1	1

AB	$A^+ B^+$		Z
	$X = 0$	$X = 1$	
00	00	01	0
01	11	01	0
11	00	10	0
10	11	01	1

14.2 More Complex Design Problems

The circuit to be designed (Mealy)

Output Z=1 if input sequence ends in either 010 or 1001

```
X=   0   0   1   0   1   0   0   1   0   0   0   1   0   0   1   1   0
                 ↑       ↑       ↑   ↑               ↑           ↑
                 a       b       c   d               e           f
Z=   0   0   0   1   0   1   0   1   1   0   0   0   1   0   1   0   0
```

14.2 More Complex Design Problems

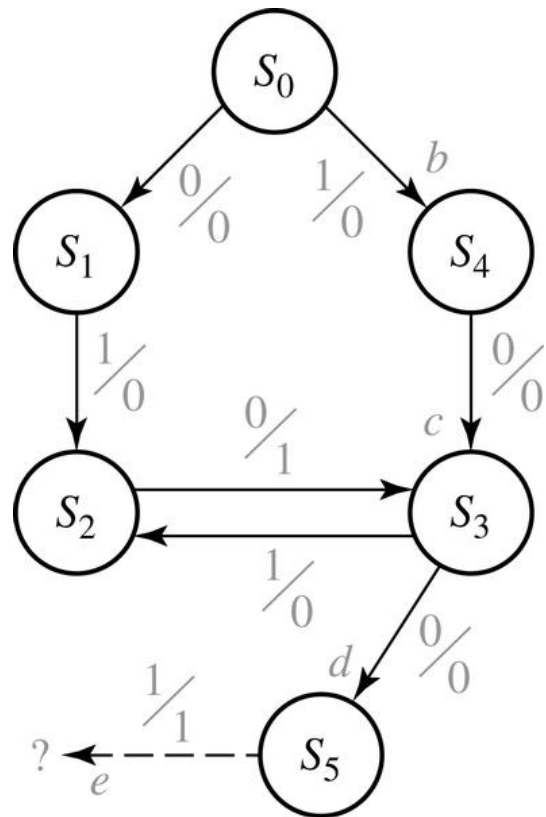Fig 14.7   formation of state graph (step1)
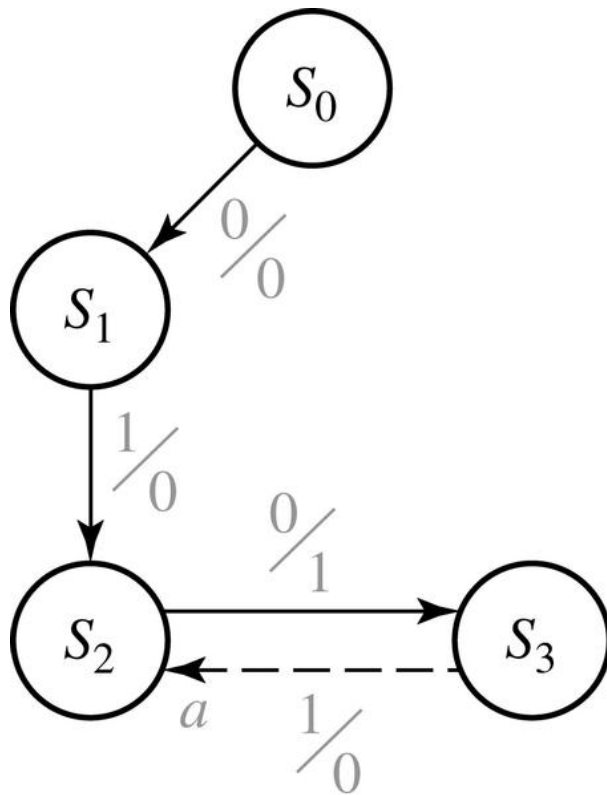
state	sequence received
S_0	reset
S_1	0
S_2	01
S_3	010

Fig 14.8   formation of state graph (step2)

state	sequence ends in
S_0	reset
S_1	0 (but not 10)
S_2	01
S_3	10
S_4	1 (but not 01)
S_5	100

Fig 14.9 Completed State Graph for a Sequence Detector to be Designed
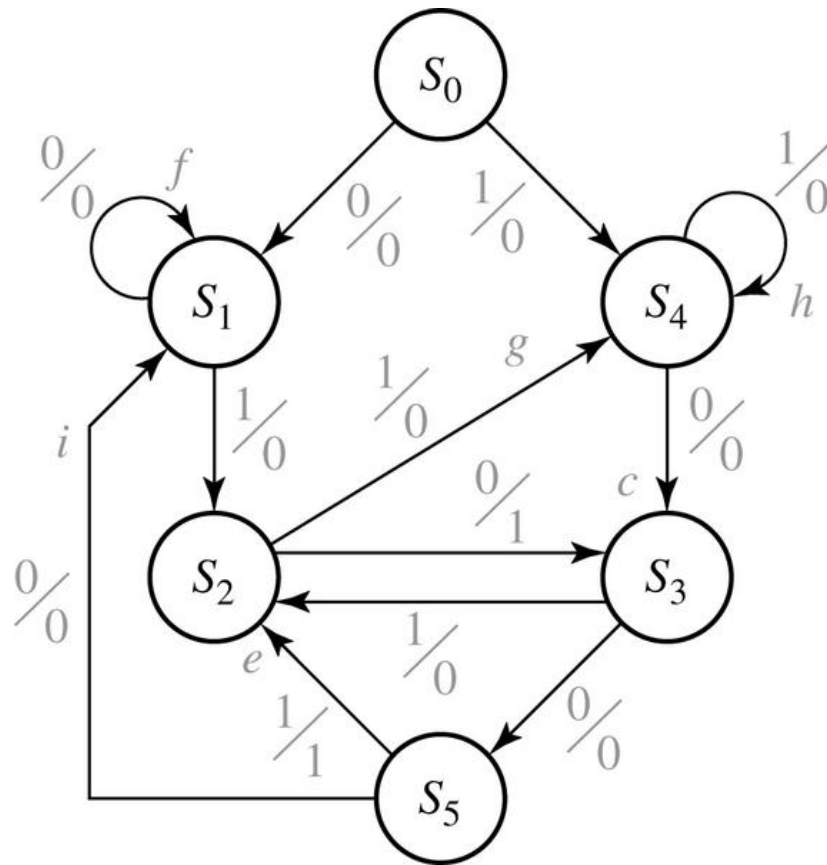
state	sequence ends in
S_0	reset
S_1	0 (but not 10)
S_2	01
S_3	10
S_4	1 (but not 01)
S_5	100

14.2 More Complex Design Problems

The circuit to be designed (Moore)

 Output Z=1 if the total number of 1's received is odd and at least two consecutive 0's have been received

X=	1	0	1	1	0	0	1	1
	↑			↑		↑	↑	↑
	a			b		c	d	e
Z=	(0)	0	0	0	0	0	1	0	1

14.2 More Complex Design Problems

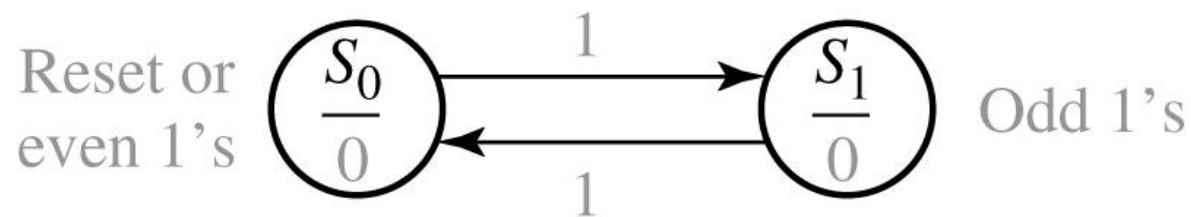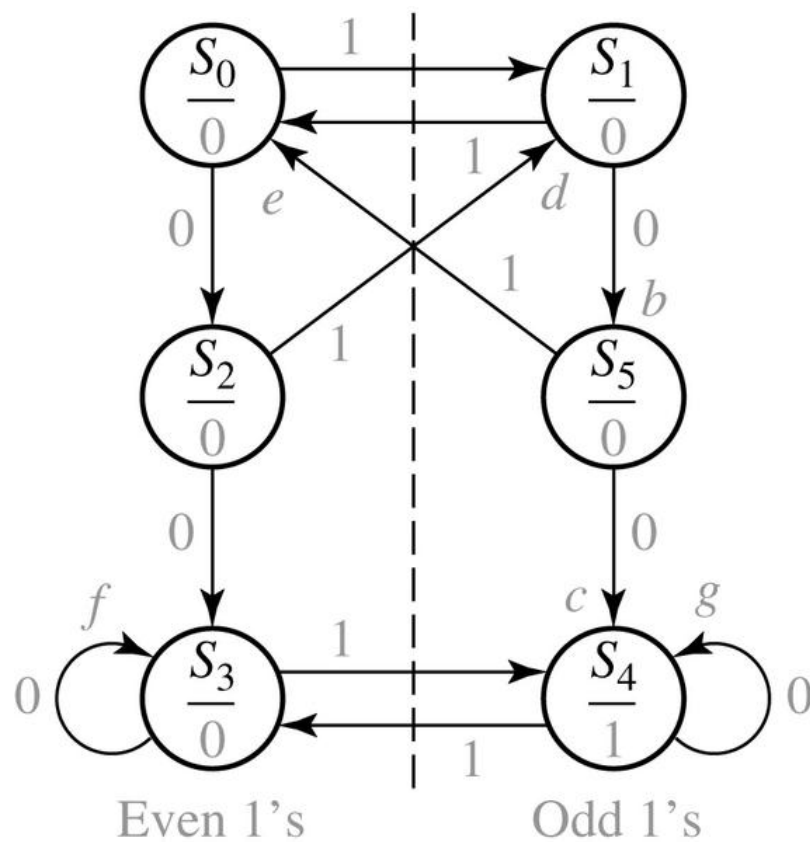Fig 14.10 formation of state graph (step1)

Fig 14.11 formation of state graph (step2)
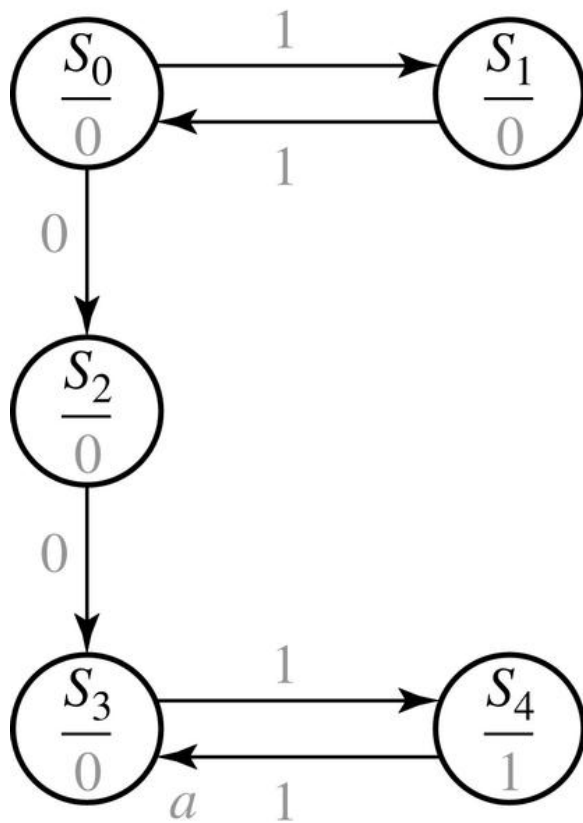
state	sequence received
S_0	reset or even 1's
S_1	odd 1's
S_2	even 1's and ends in 0
S_3	even 1's and 00 has occurred
S_4	00 has occurred and odd 1's

Fig 14.12 Completed State Graph for a Sequence Detector to be Designed

state	Input sequences
S_0	reset or even 1's
S_1	odd 1's
S_2	even 1's and ends in 0
S_3	even 1's and 00 has occurred
S_4	odd 1's and 00 has occurred
S_5	odd 1's and ends in 0

14.3   Guidelines for Construction of State Graphs

1.   Construct some sample input and output sequences to make sure that you understand the problem statement.

2. Determine under what conditions ,if any, the circuit should reset to its initial state.

3. If only one or two sequences lead to a non-zero output, a good way   to start is to construct a partial state graph for those sequences.

4. Determine what sequences or groups of sequences must be remembered by the circuit and set up states accordingly.

5. Each time you add an arrow to the state graph, determine it can go to one of the previously defined states or whether a new state must be added

6. Check your state graph to make sure there is one and only one path leaving each state for each combination of values of the input variables

7. When your state graph is complete, test it by applying the input sequences formulated in part1 and making sure the output sequences are correct

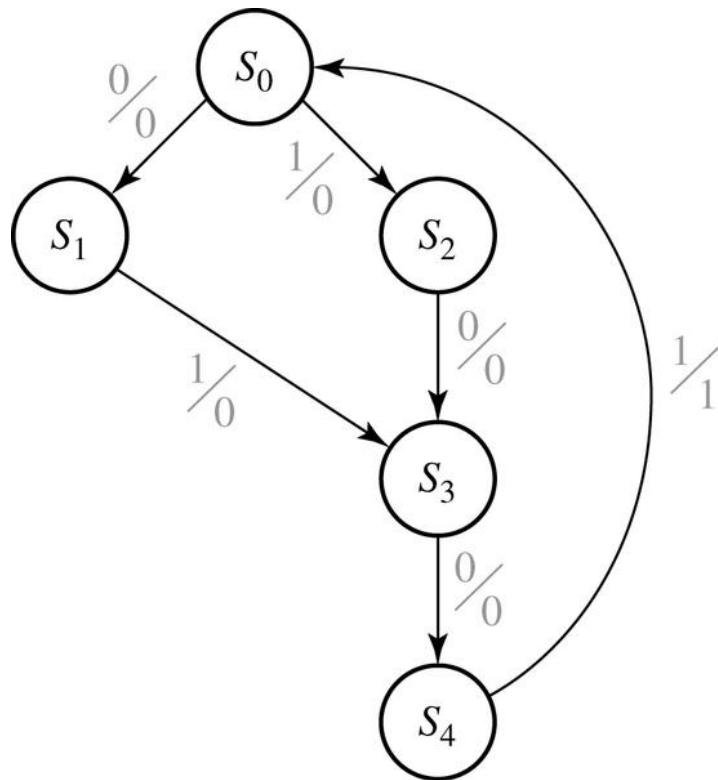Example 1 : Z=1 when input sequence 0101 or 1001 occurs.

The circuit resets after every four inputs. Mealy Circuit

A typical sequence of input and output

X =	0101	0010	1001	0100
Z =	0001	0000	0001	0000

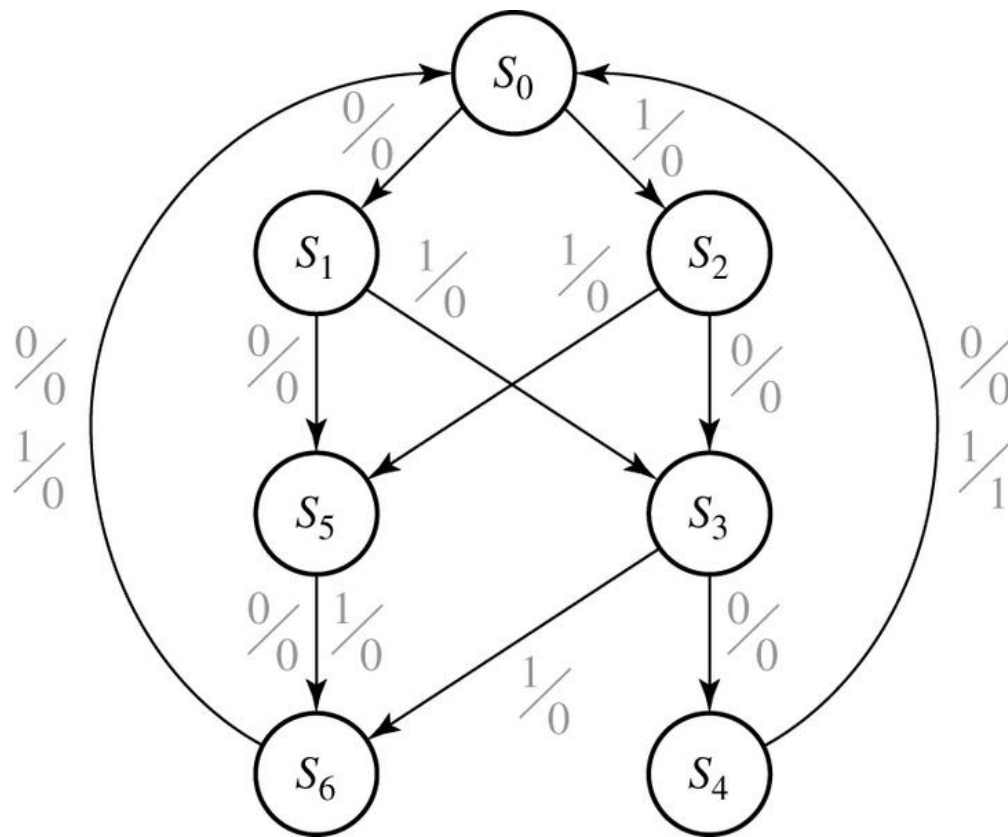# 14.3 Guidelines for Construction of State Graphs

Fig 14.13 Partial State Graph for Example 1

state	sequence received
S_0	Reset
S_1	0
S_2	1
S_3	01 or 10
S_4	010 or 100

Fig 14.14 Complete State Graph for Example 1

state	sequence received
S_0	Reset
S_1	0
S_2	1
S_3	01 or 10
S_4	010 or 100
S_5	two inputs received, no 1 output is possible
S_6	three inputs received, no 1 output is possible

Example 2 : Z1=1 every time the input sequence 100 is completed

Z2=1 every time the input sequence 010 is completed

Once Z2=1 occurred, Z1=1 can never occur but not vice versa

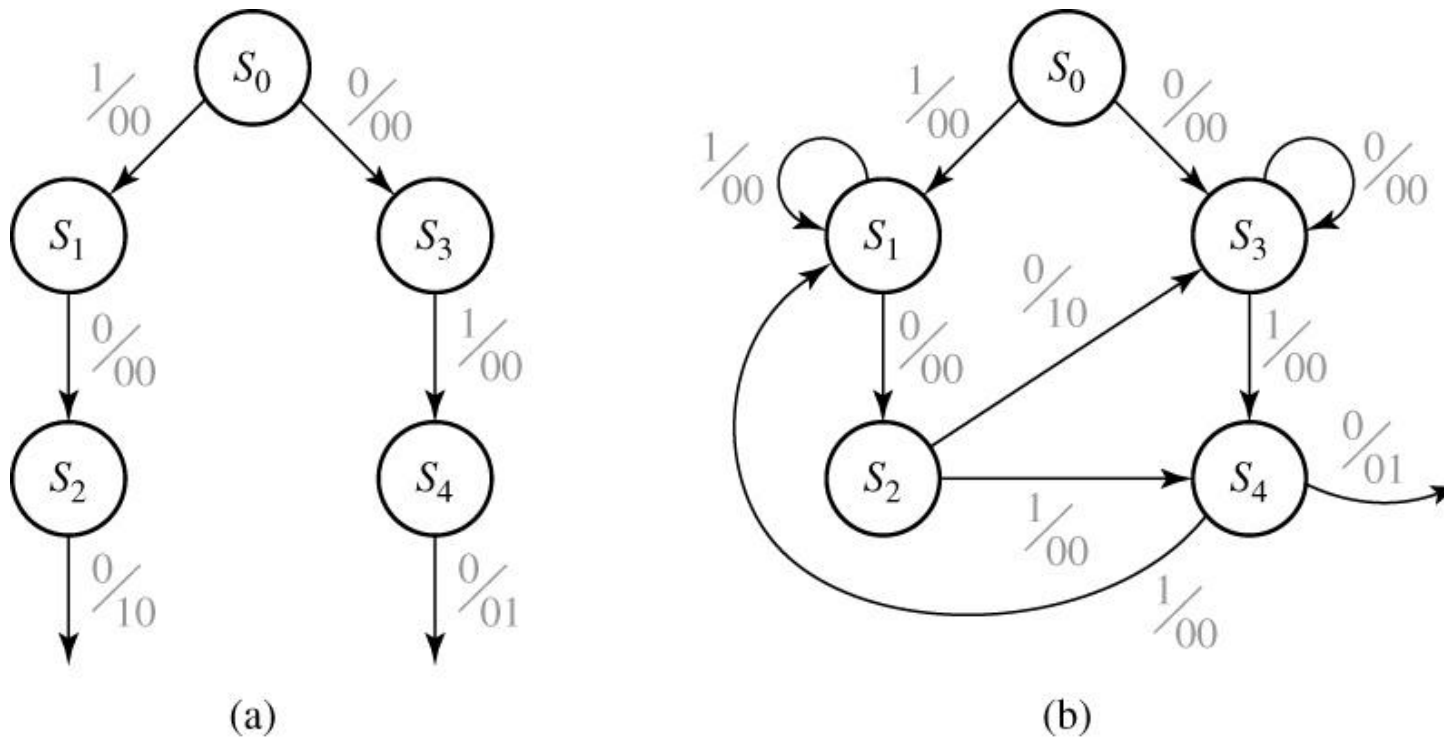Mealy circuit

A typical sequence of input and output

$$X = 1\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 0\ |\ 1\ 0\ 1\ 0\ 0\ 1\ 0\ 1\ 1\ 0\ 1\ 0\ 0$$

$$Z_1 = 0\ 0\ 1\ 0\ 0\ 0\ 1\ 0\ 0\ |\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0$$

$$Z_2 = 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1\ |\ 0\ 1\ 0\ 1\ 0\ 0\ 1\ 0\ 0\ 0\ 0\ 1\ 0$$

Fig 14.15 Partial Graphs for Example 2

(a)   (b)
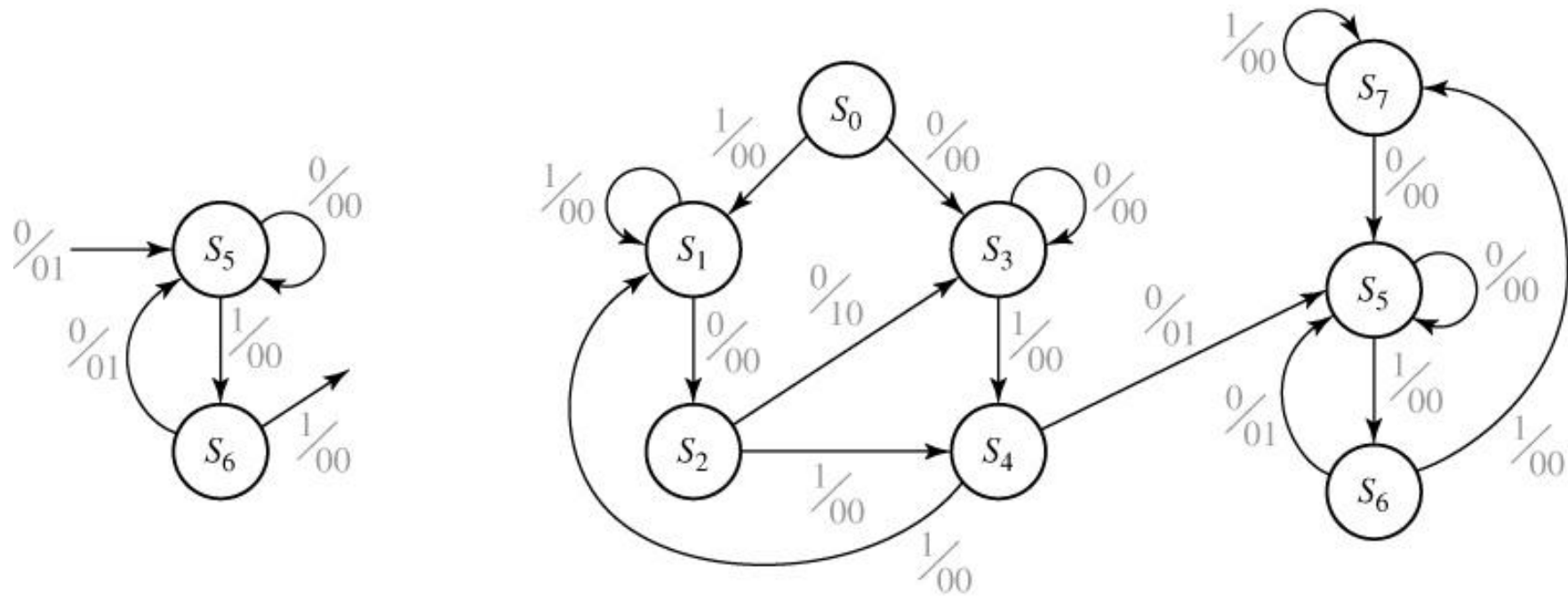
14.3 Guidelines for Construction of State Graphs

Table 14−5 State Descriptions for Example 2

stats	Description		
S_0	No progress on 100	No progress on 010	
S_1	Progress of 1 on 100	No progress on 010	
S_2	Progress of 10 on 100	Progress of 0 on 010	010 has never occurred
S_3	No progress on 100	Progress of 0 on 010	
S_4	Progress of 10 on 100	Progress of 01 on 010	
S_5		Progress of 0 on 010	
S_6		Progress of 01 on 010	010 has occurred
S_7		No progress on 010	

Fig 14.16 State Graphs for Example 2

(a) Partial graph for 010

(b) Complete state graph

14.3 Guidelines for Construction of State Graphs

Table 14-6

Present state	Next State $X = 0$	State $X = 1$	Output $X = 0$	$(Z_1 Z_2)$ $X = 1$
S_0	S_3	S_1	00	00
S_1	S_2	S_1	00	00
S_2	S_3	S_4	10	00
S_3	S_3	S_4	00	00
S_4	S_5	S_1	01	00
S_5	S_5	S_6	00	00
S_6	S_5	S_7	01	00
S_7	S_5	S_7	00	00

14.3 Guidelines for Construction of State Graphs

Example 3: Two inputs – X1, X2, One output – Z

    (a) The input sequence X1X2=01, 11 cause the output 0

    (b) The input sequence X1X2=10, 11 cause the output 1

    (c) The input sequence X1X2=10, 01 cause the output to change

Previous Input (X_1X_2)	Output (Z)	State Designation
00 or 11	0	S_0
00 or 11	1	S_1
01	0	S_2
01	1	S_3
10	0	S_4
10	1	S_5

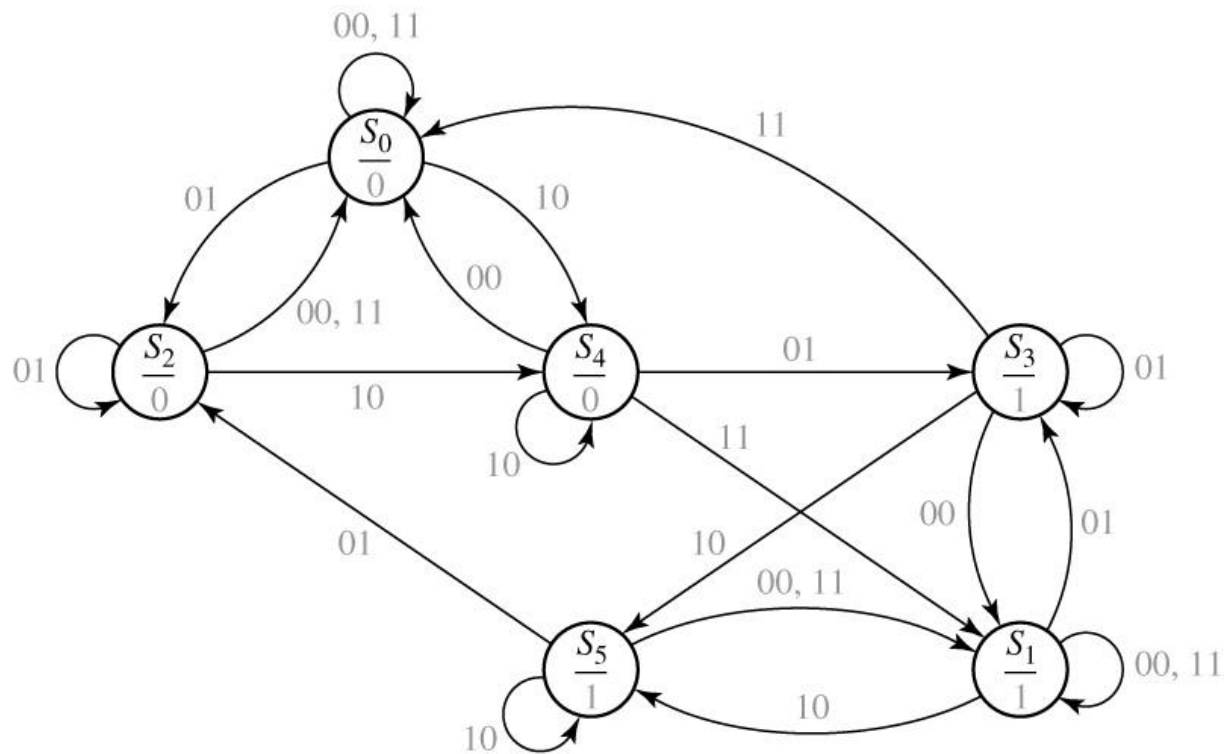# 14.3 Guidelines for Construction of State Graphs

Table 14-7

Present State	Z	$X_1X_2 =$	00	01	11	10
			Next state			
S_0	0		S_0	S_2	S_0	S_4
S_1	1		S_1	S_3	S_1	S_5
S_2	0		S_0	S_2	S_0	S_4
S_3	1		S_1	S_3	S_0	S_5
S_4	0		S_0	S_3	S_1	S_4
S_5	1		S_1	S_2	S_1	S_5

14.3 Guidelines for Construction of State Graphs
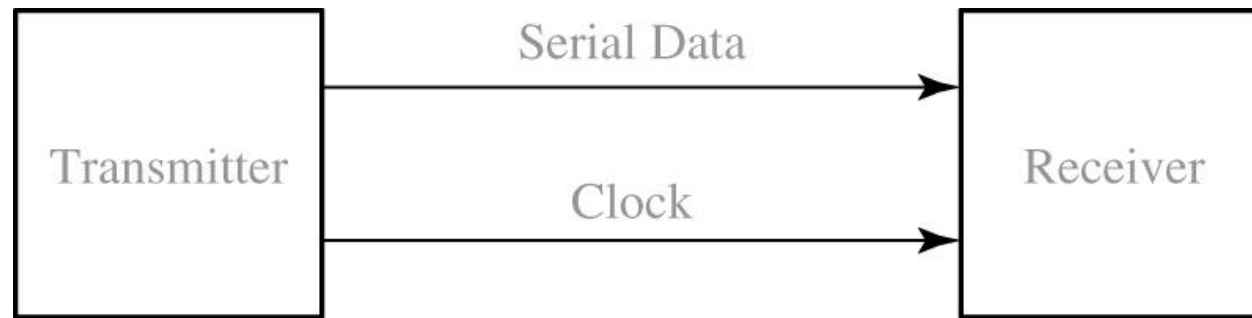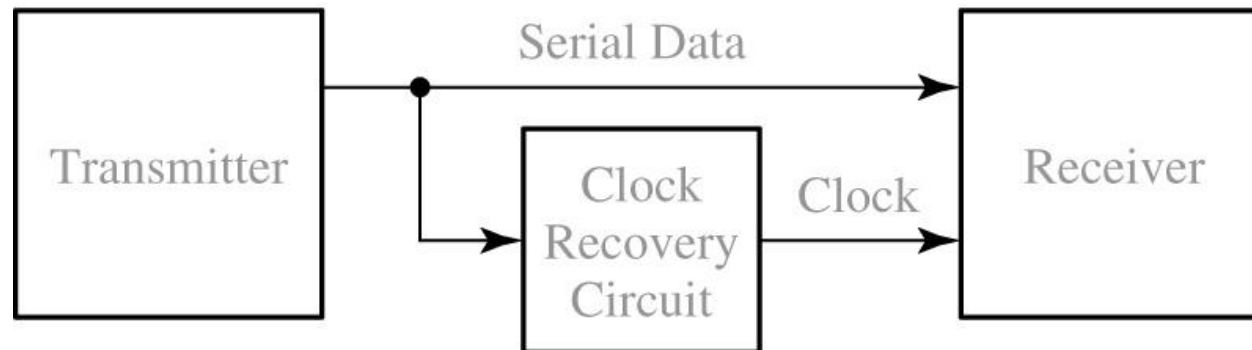
Fig 14-17 State Graph for Example 3

14.4 Serial Data Code Conversion
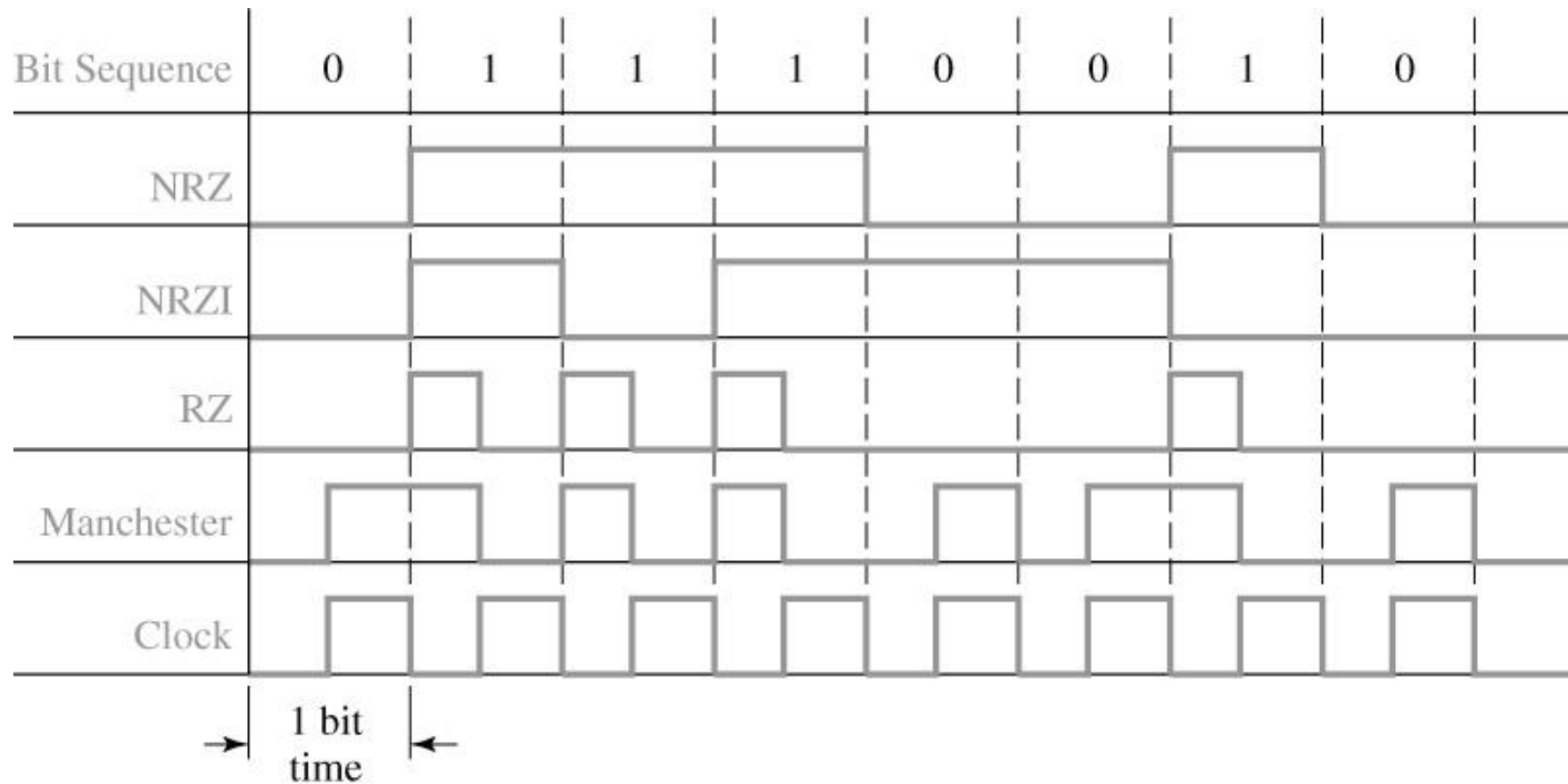
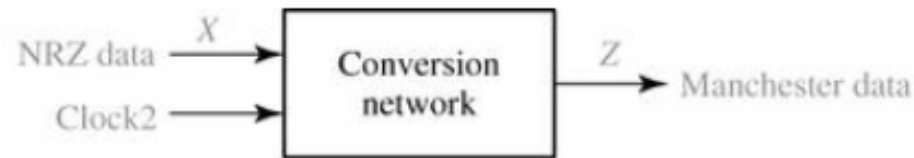Fig 14.18 Serial Data Transmission

(a)

(b)

14.4 Serial Data Code Conversion

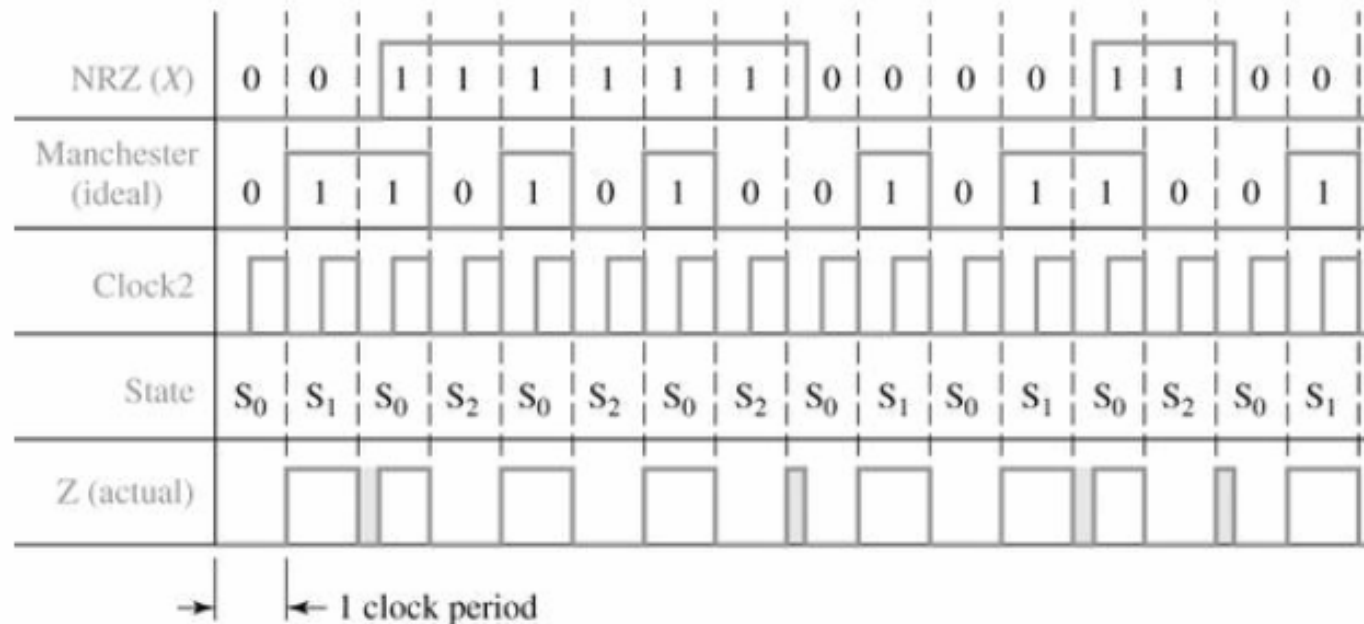Fig 14.19 Coding Schemes for Serial Data Transmission

14.4 Serial Data Code Conversion

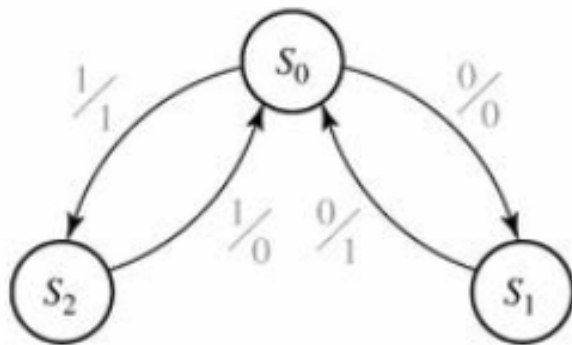Fig 14.20 Mealy circuit for NRZ to Manchester Conversion

(a) Conversion network

(b) Timing chart

14.4 Serial Data Code Conversion
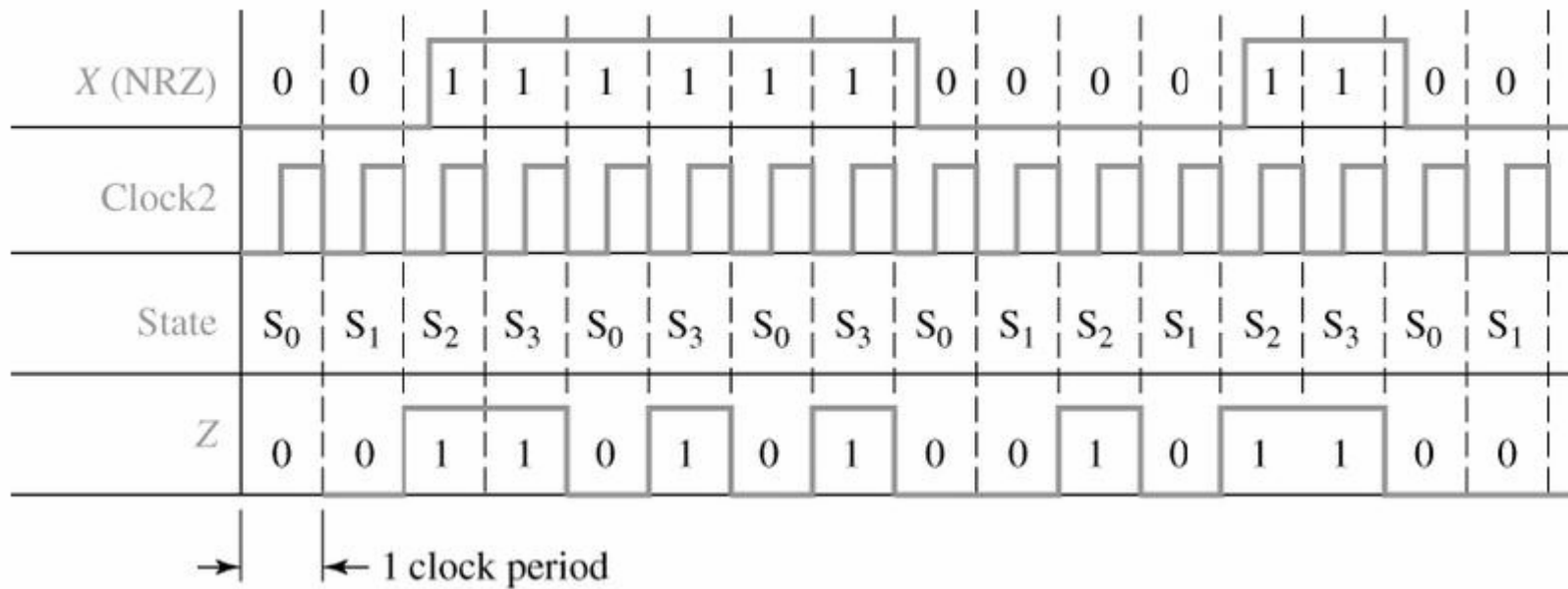
Fig 14.20 Sequence Detector to be Designed

(c) State graph

Present	Next State		Output (Z)	
State	X = 0	X = 1	X = 0	X = 1
S_0	S_1	S_2	0	1
S_1	S_0	-	1	-
S_2	-	S_0	-	0

(d) State table

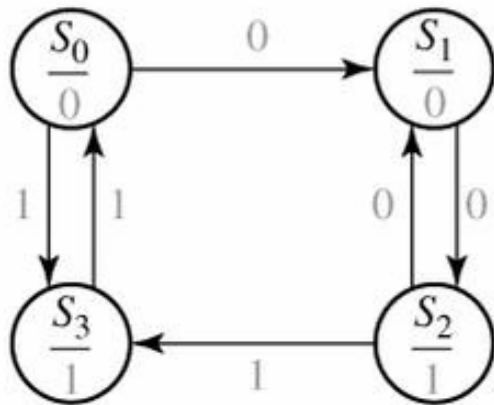# 14.4 Serial Data Code Conversion

Fig 14.21 Moore Circuit for NRZ-to-Manchester Conversion

(a) Timing chart

14.4 Serial Data Code Conversion

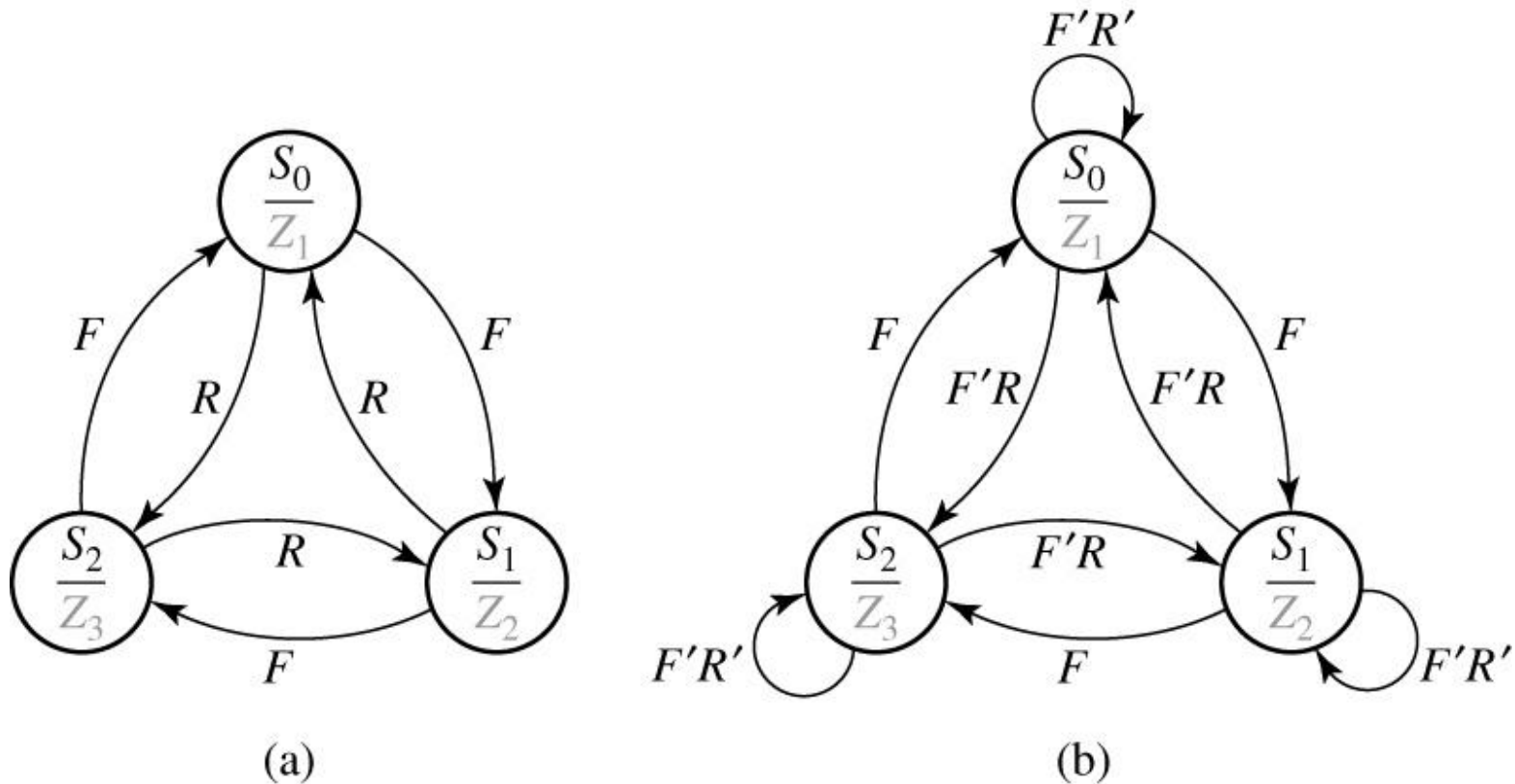Fig 14.21 Moore Circuit for NRZ–to–Manchester Conversion

(b) State graph

Present State	Next State		Present Output (Z)
	$X = 0$	$X = 1$	
S_0	S_1	S_3	0
S_1	S_2	-	0
S_2	S_1	S_3	1
S_3	-	S_0	1

(c) State table

14.5 Alphanumeric State Graph Notation

Fig 14.22 State Graphs with Variable Names on Arc Labels

(a)

(b)

14.5 Alphanumeric State Graph Notation

Table 14-8 State Table for Fig 14-22

PS	NS				Output		
	FR = 00	01	10	11	Z_1	Z_2	Z_3
S_0	S_0	S_2	S_1	S_1	1	0	0
S_1	S_1	S_0	S_2	S_2	0	1	0
S_2	S_2	S_1	S_0	S_0	0	0	1

The result : $F + F'R + F'R' = F + F' = 1$

If we AND together every possible pair of arc labels emanating from S_0, we get

$$F \cdot F'R = 0, \qquad F \cdot F'R' = 0, \qquad F'R \cdot F'R' = 0,$$