# CHAPTER 13

## Analysis of Clocked Sequential Circuit

# Contents

# Objectives

Topics introduced in this chapter:

13.1 Analyze a sequential circuit by signal tracing.

13.2 Given a sequential circuit, write the next-state equations for the flip-flops and derive the state graph or state table. Using the state graph, determine the state sequence and output sequence for a given input sequence .

13.3 Explain the difference between a Mealy machine and a Moore machine.

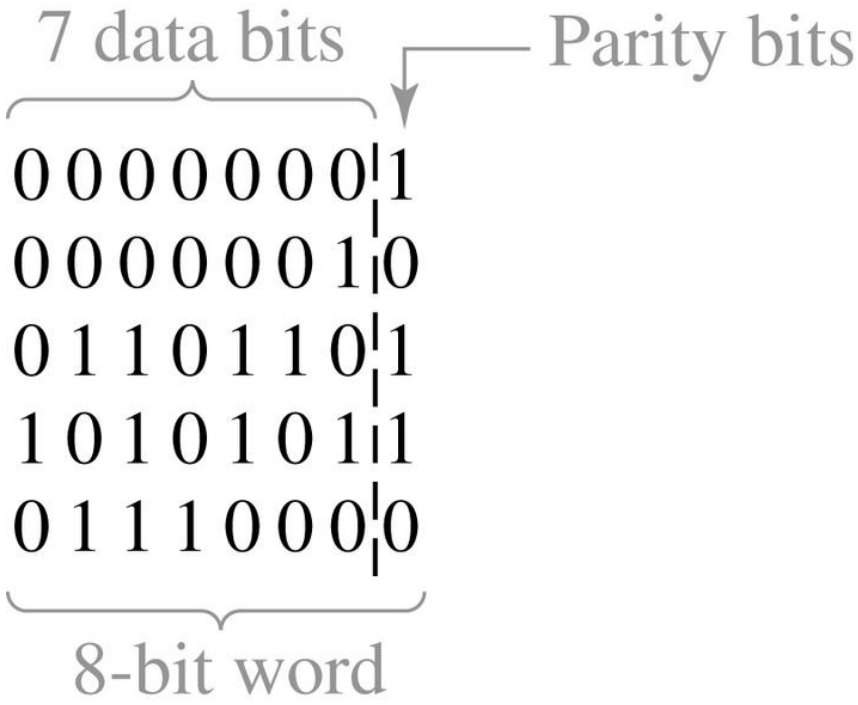
13.4 Given a state table, construct the corresponding state graph, and conversely.

13.5 Given a sequential circuit or a state table and an input sequence, draw a timing chart for the circuit. Determine the output sequence from the timing chart, neglecting any false outputs.

13.6 Draw a general model for a clocked Mealy or Moore sequential circuit. Explain the operation of the circuit in terms of these models. Explain why a clock is needed to ensure proper operation of the circuit.

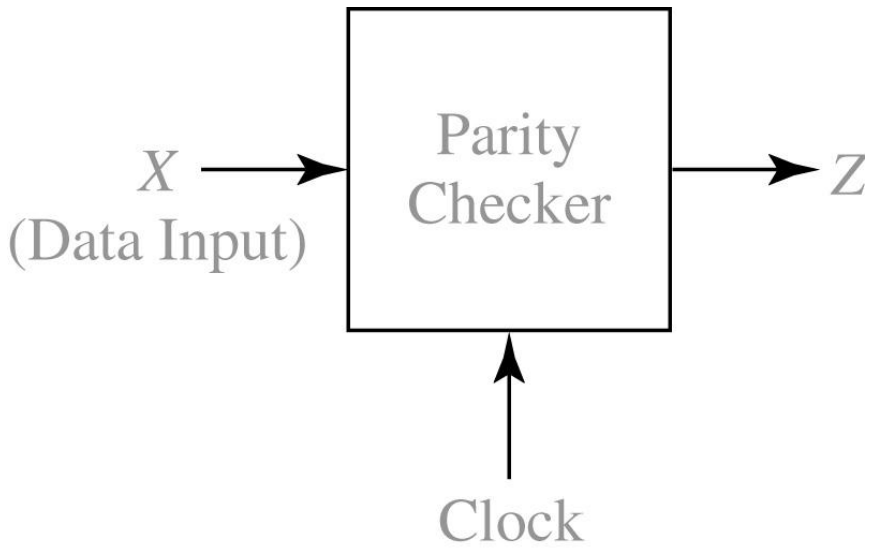
# 13.1 A Sequential Parity Checker

8-bit words with odd parity



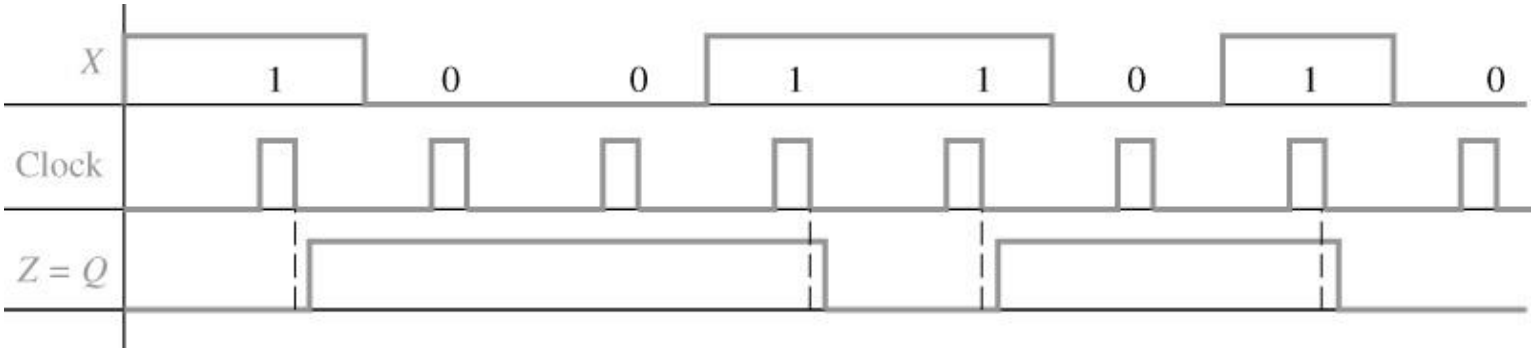
# 13.1 A Sequential Parity Checker

Fig 13-1. Block Diagram for Parity Checker



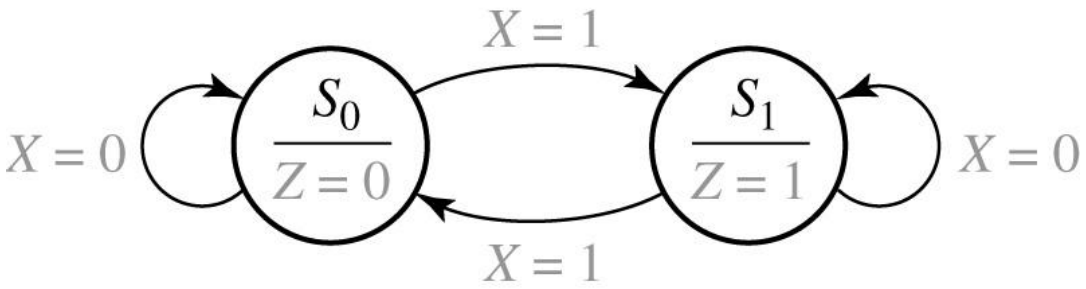
# 13.1 A Sequential Parity Checker

Figure 13-2: Waveforms for Parity Checker



# 13.1 A Sequential Parity Checker

Figure 13-3: State Graph for Parity Checker (Moore Machine)



# 13.1 A Sequential Parity Checker

Table 13-1. State Table for Parity Checker

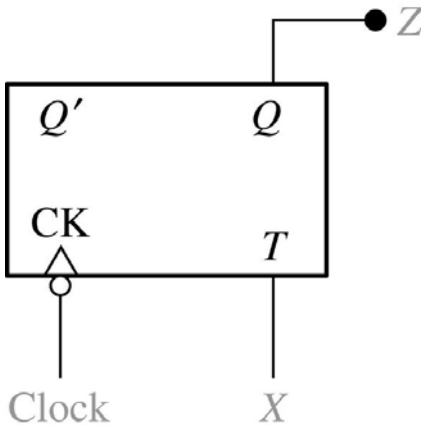
| Present State | Next state $X=0$ | Next state $X=1$ | Present Output |
|---|---|---|---|
| $S_0$ | $S_0$ | $S_1$ | 0 |
| $S_1$ | $S_1$ | $S_0$ | 1 |

(a)

| $Q$ | $Q^+$ $X=0$ | $Q^+$ $X=1$ | $T$ $X=0$ | $T$ $X=1$ | $Z$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |

(b)

Figure 13-4: Parity Checker

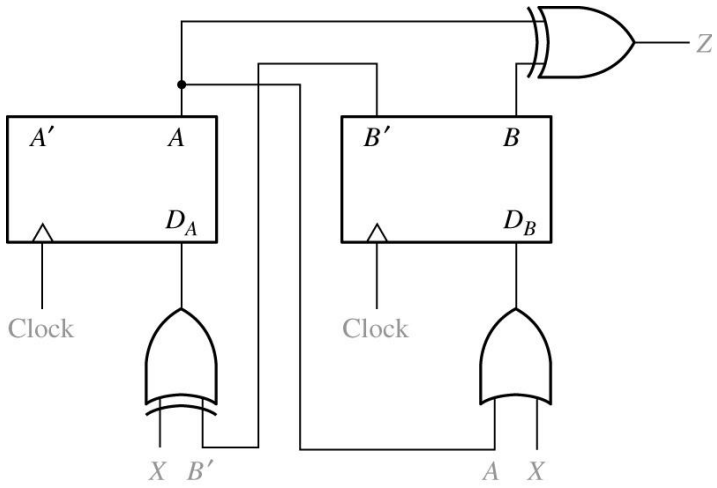


# 13.2 Analysis by Signal Tracing

**Output tracing**

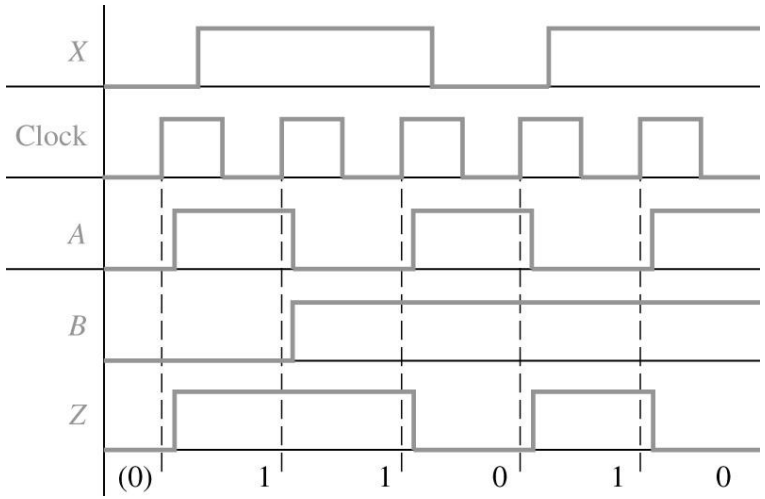
1. **Assume an initial state of F/F**
2. **For the first input in the give sequence, determine the output and F/F inputs**
3. **Determine the new sets of F/F states after the next active clock edge**
4. **Determine the output that corresponds to the new states**
5. **Repeat 2,3,4 for each input in the given sequence**

Figure 13-5: Moore Sequential Circuit to be Analyzed



# 13.2 Analysis by Signal Tracing

Figure 13-6: Timing Chart for Figure 13-5




X = 0 1 1 0 1

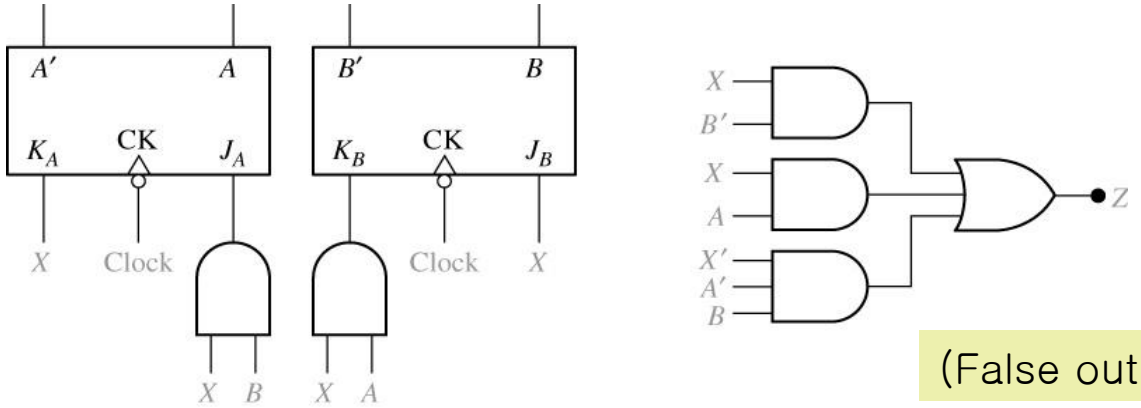
A = 0 1 0 1 0 1

B = 0 0 1 1 1 1

Z = (0) 1 1 0 1 0

# 13.2 Analysis by Signal Tracing

Figure 13-7: Mealy Sequential Circuit to be Analyzed




X = 1 0 1 0 1

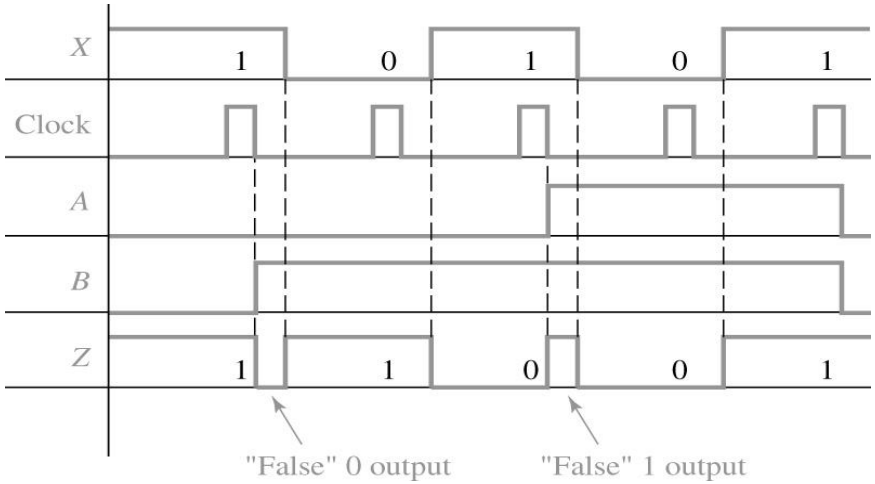
A = 0 0 0 1 1 0

B = 0 1 1 1 1 0

Z = 1(0) 1 0(1) 0 1

(False outputs are indicated in parentheses)

Figure 13-8: Timing Chart for Circuit of Figure 13-7



# 13.3 State Table and Graphs

1. Determine the flip-flop input equations and the output equations from the circuit

2. Derive the next-state equation for each flip-flop from its input equations, using one of the following relations:

| | | |
|---|---|---|
| D flip-flop | $Q^+ = D$ | (13-1) |
| D-CE flip-flop | $Q^+ = D \cdot CE + QCE'$ | (13-2) |
| T-flip-flop | $Q^+ = T \oplus Q$ | (13-3) |
| S-R flip-flop | $Q^+ = S + R'Q$ | (13-4) |
| J-K flip-flop | $Q^+ = JQ' + K'Q$ | (13-5) |

3. Plot a next-state map for the flip-flop.

4. Combine these maps to form the state table. Such a state table, which gives the next state of the flip-flops as a function of their present state and the circuit inputs, is frequently referred to as a transition table.

# 13.3 State Table and Graphs

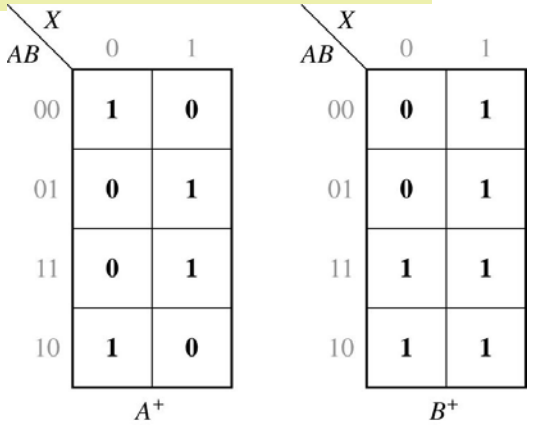
1. The flip-flop input equations and output equation are

$$D_A = X \oplus B' \qquad D_B = X + A \qquad Z = A \oplus B$$

2. The next-state equations for the flip-flops are

$$A' = X \oplus B' \qquad B^+ = X + A$$

3. The corresponding maps are




4. Combining these maps yields the transition table in Table 13-2(a), which gives the next state of both flip-flops (A+,B+) as a function of the present state and input. The output function Z is then added to the table. In this example, the output depends only on the present state of the flip-flops and not on the input,so only a single output column is required

# 13.3 State Table and Graphs

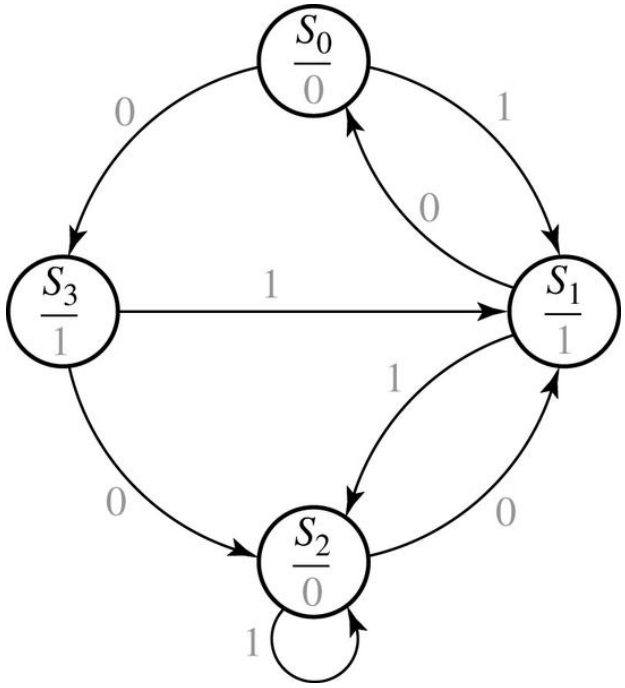
Table 13-2: Moore State Tables for Figure 13-5

| $AB$ | $A^+B^+$ $X=0$ | $X=1$ | $Z$ |
|---|---|---|---|
| 00 | 10 | 01 | 0 |
| 01 | 00 | 11 | 1 |
| 11 | 01 | 11 | 0 |
| 10 | 11 | 01 | 1 |

| Present State | Next state $X=0$ | $X=1$ | Present Output(z) |
|---|---|---|---|
| $S_0$ | $S_3$ | $S_1$ | 0 |
| $S_1$ | $S_0$ | $S_2$ | 1 |
| $S_2$ | $S_1$ | $S_2$ | 0 |
| $S_3$ | $S_2$ | $S_1$ | 1 |

# 13.3 State Table and Graphs

Figure 13-9: Moore State Graph for Figure 13-5



# 13.3 State Table and Graphs

The state table and graph for the Mealy machine of Figure 13-7.
The next-state and output equations are

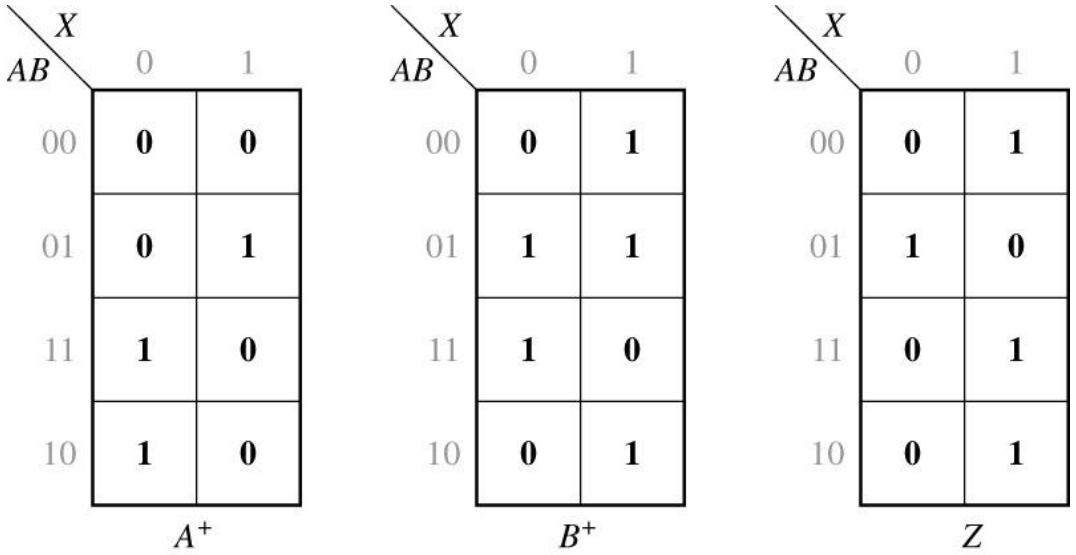
$$A^{+} = J_A A' + K_A' A = XBA' + X'A$$

$$B^{+} = J_B B' + K_B' B = XB' + (AX)'B = XB' + X'B + A'B$$

$$Z = X'A'B + XB' + XA$$

# 13.3 State Table and Graphs

Figure 13-10



| $AB$ \ $X$ | 0 | 1 |
|---|---|---|
| 00 | **0** | **0** |
| 01 | **0** | **1** |
| 11 | **1** | **0** |
| 10 | **1** | **0** |

$A^+$

| $AB$ \ $X$ | 0 | 1 |
|---|---|---|
| 00 | **0** | **1** |
| 01 | **1** | **1** |
| 11 | **1** | **0** |
| 10 | **0** | **1** |

$B^+$

| $AB$ \ $X$ | 0 | 1 |
|---|---|---|
| 00 | **0** | **1** |
| 01 | **1** | **0** |
| 11 | **0** | **1** |
| 10 | **0** | **1** |

$Z$

# 13.3 State Table and Graphs

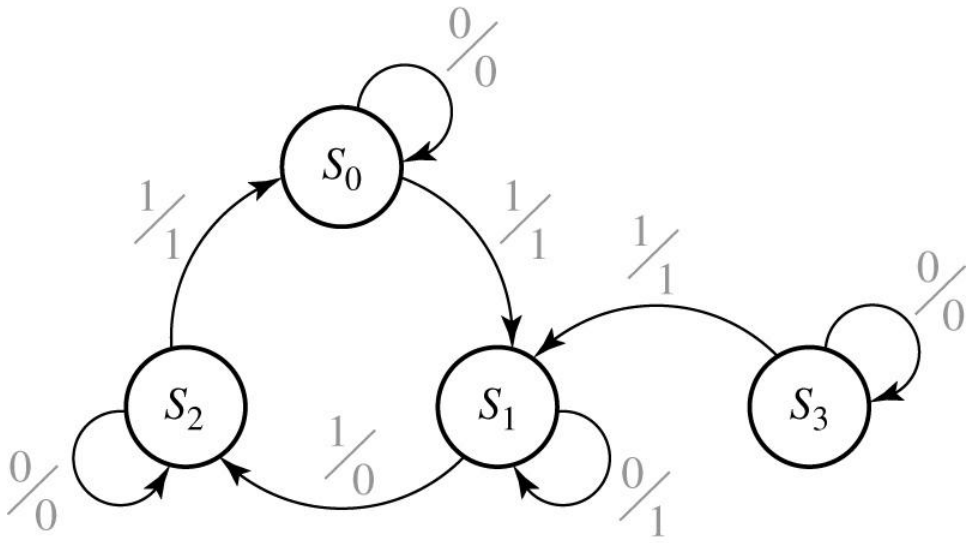
Table 13-3 Mealy State Tables for Figure 13-7

| $AB$ | $A^+B^+$ $X=0$ | $A^+B^+$ $X=1$ | $Z$ $X=0$ | $Z$ 1 |
|---|---|---|---|---|
| 00 | 00 | 01 | 0 | 1 |
| 01 | 01 | 11 | 1 | 0 |
| 11 | 11 | 00 | 0 | 1 |
| 10 | 10 | 01 | 1 | 1 |

| Present State | Next state $X=0$ | Next state $X=1$ | Present Output(z) $X=0$ | Present Output(z) $X=1$ |
|---|---|---|---|---|
| $S_0$ | $S_0$ | $S_1$ | 0 | 1 |
| $S_1$ | $S_1$ | $S_2$ | 1 | 0 |
| $S_2$ | $S_2$ | $S_0$ | 0 | 1 |
| $S_3$ | $S_3$ | $S_1$ | 0 | 1 |

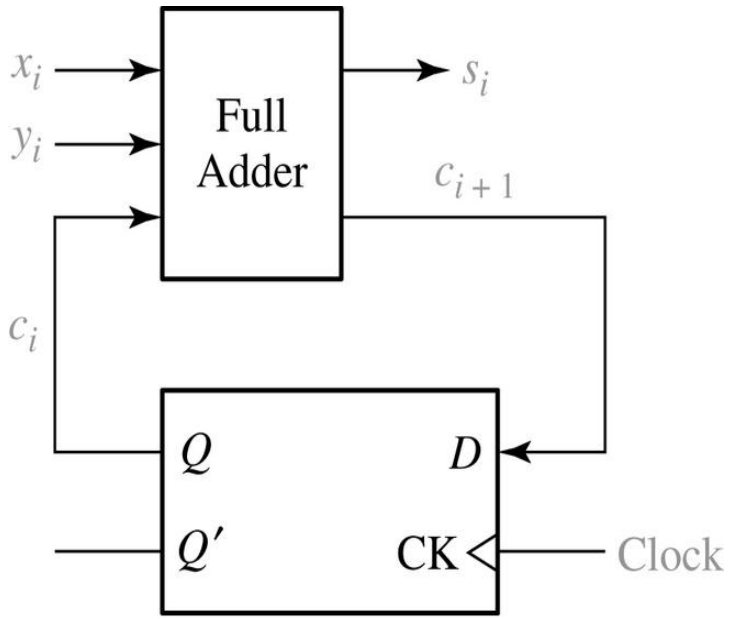
# 13.3 State Table and Graphs

Figure 13-11: Mealy State Graph for Figure 13-7



# 13.3 State Table and Graphs

Figure 13-12: Serial Adder



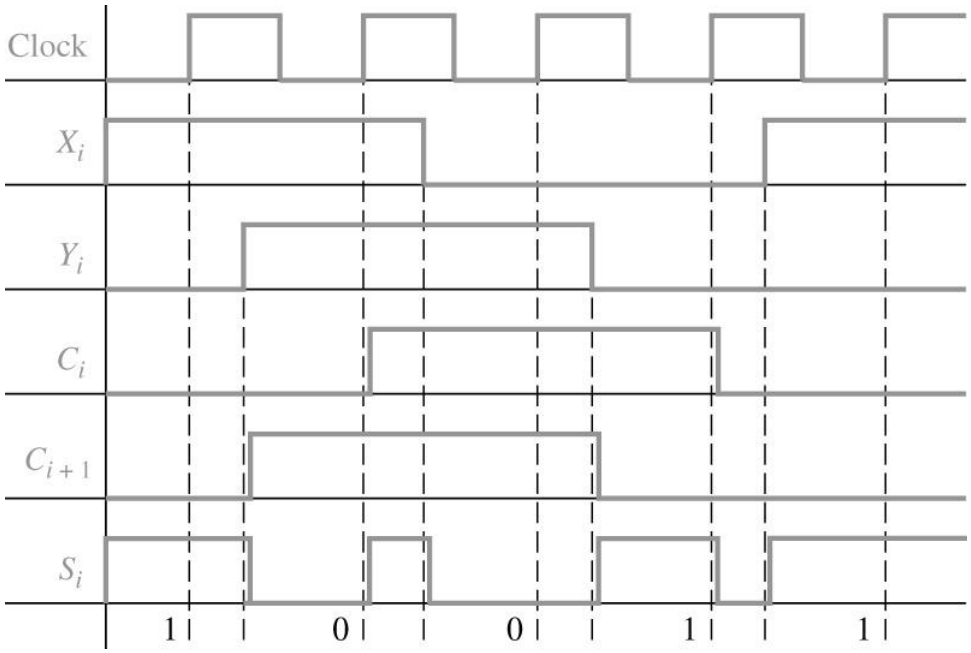

(a) With *D* flip-flop

| $x_i$ | $y_i$ | $c_i$ | $c_{i+1}$ | $s_i$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

(b) Truth table

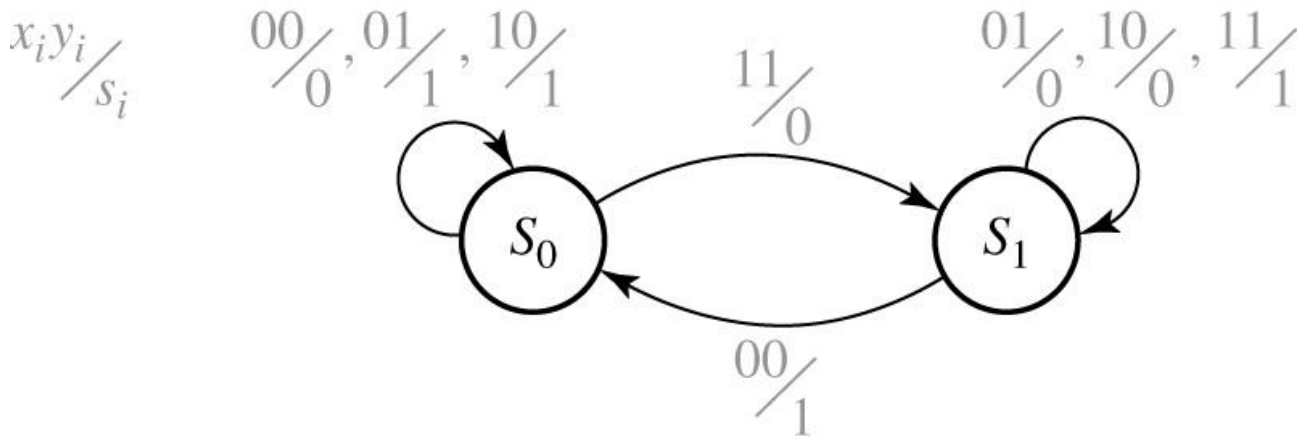
# 13.3 State Table and Graphs

Figure 13-13: Timing Diagram for Serial Adder



# 13.3 State Table and Graphs

Figure 13-14: State Graph for Serial Adder



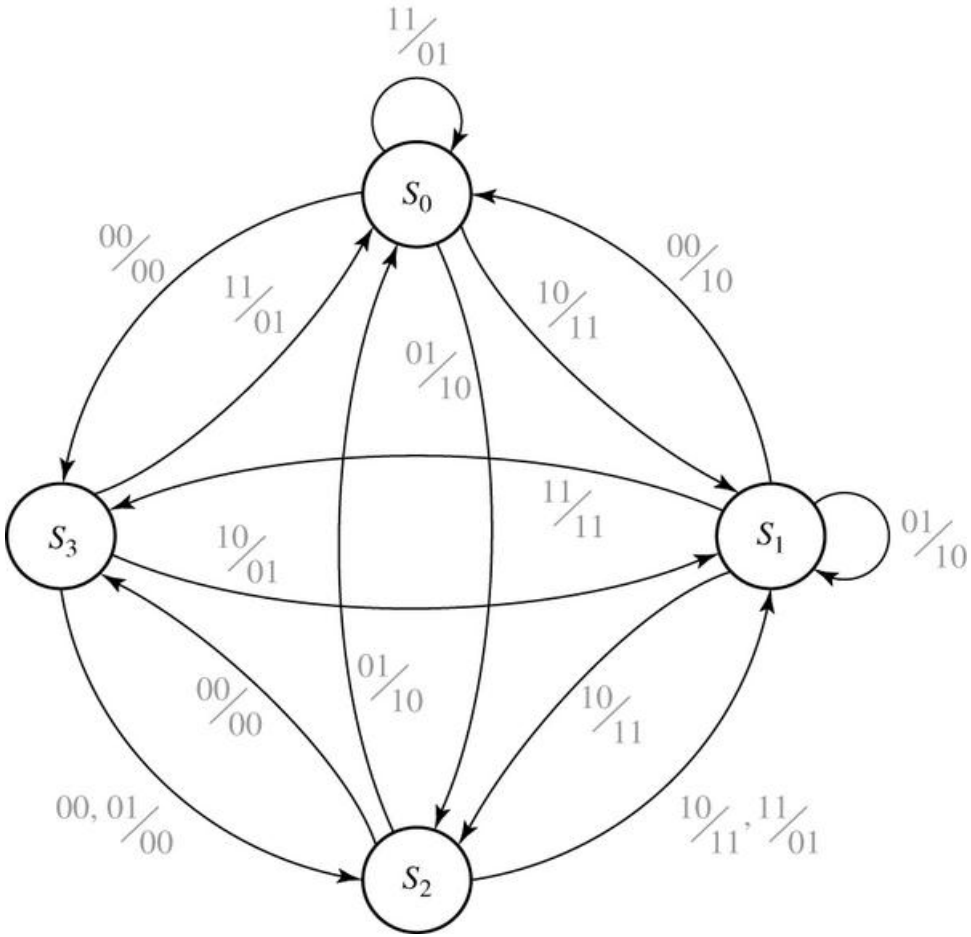
# 13.3 State Table and Graphs

Table 13-4 A Stable with Multiple Inputs and Outputs

| Present State | Next state | | | | Present Output(z) | | | |
|---|---|---|---|---|---|---|---|---|
| | $X_1X_2 = 00$ | 01 | 10 | 11 | $X_1X_2 = 00$ | 01 | 10 | 11 |
| $S_0$ | $S_3$ | $S_2$ | $S_1$ | $S_0$ | 00 | 10 | 11 | 01 |
| $S_1$ | $S_0$ | $S_1$ | $S_2$ | $S_3$ | 10 | 10 | 11 | 11 |
| $S_2$ | $S_3$ | $S_0$ | $S_1$ | $S_1$ | 00 | 10 | 11 | 01 |
| $S_3$ | $S_2$ | $S_2$ | $S_1$ | $S_0$ | 00 | 00 | 01 | 01 |

# 13.3 State Table and Graphs

Figure 13-15: State Graph for Table 13-4



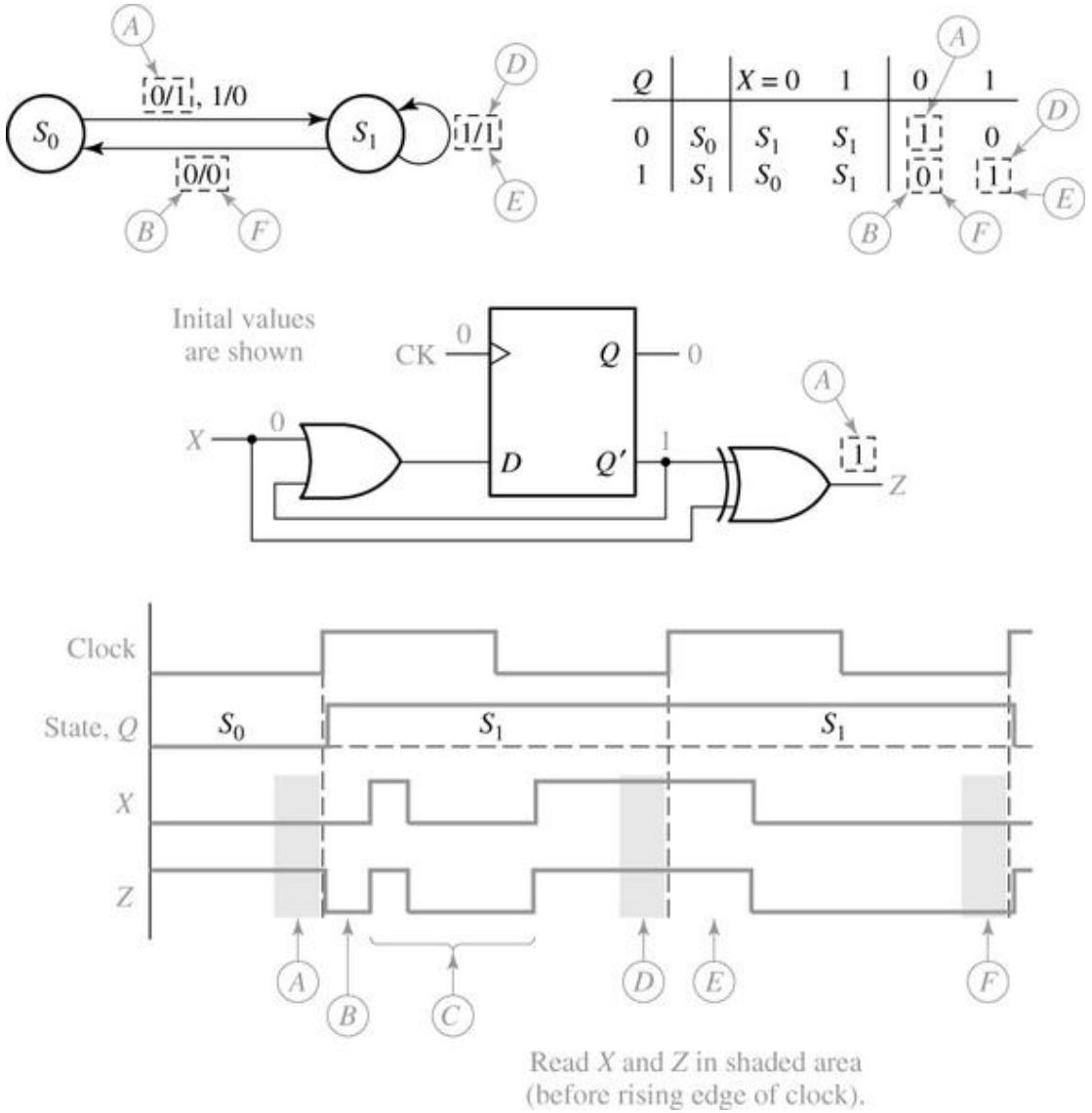
# 13.3 State Table and Graphs

## Construction and interpretation of Timing Chart

1. When constructing timing charts, note that a state change can only occur after the rising (or falling) edge of the clock, depending on the type of flip-flop used.
2. The input will normally be stable immediately before and after the active clock edge.
3. For a Moore circuit, the output can change only when the state changes, but for a Mealy circuit, the output can change when the input changes as well as when the state changes. A false may occur between the state changes and the time the input is changed to its new value. ( In other words, if the state has changed to its next value, but the old input is still present, the output may be temporally incorrect.)
4. False outputs are difficult to determine from the state graph, so use either signal tracing through the circuit or use the state table when constructing timing charts for Mealy circuit.
5. When using a Mealy state table for constructing timing charts, the procedure is as follows:
   a) for the first input, read the present output and plot it.
   b) Read the next state and plot it (following the active edge of the clock pulse).
   c) Go to the row in the table which corresponds to the next state and read the output under the old input column and plot it
   d) Change to the next input and repeat step (a) (b) and ( c).
6. For Mealy circuits, the best time to read the output is just before the active edge of the clock, because the output should always be correct at that time.

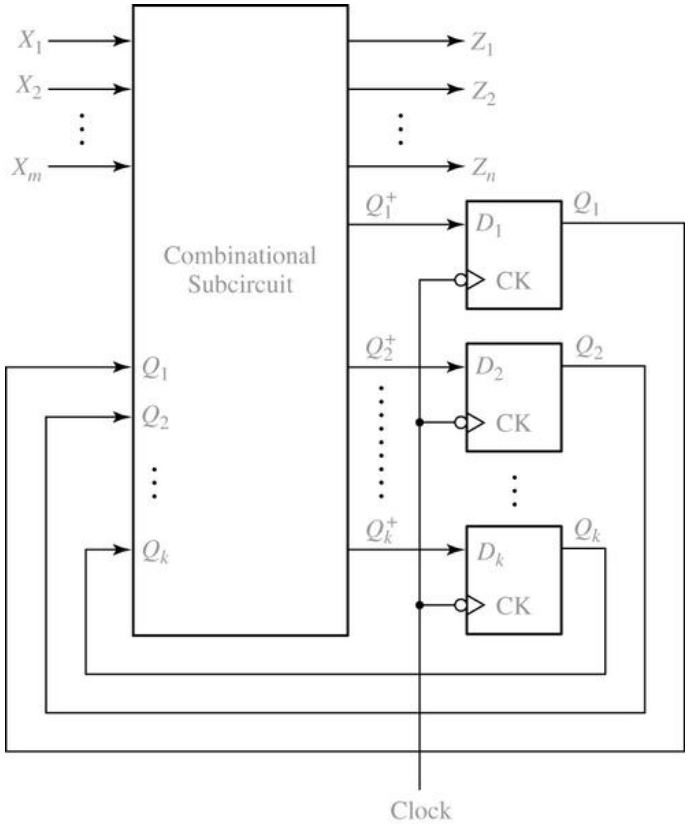
# 13.3 State Table and Graphs

Figure 13-16



# 13.4 General Models for Sequential Circuit

Figure 13-17: General Model for Mealy Circuit Using ClockedD Flip-Flops



# 13.4 General Models for Sequential Circuit

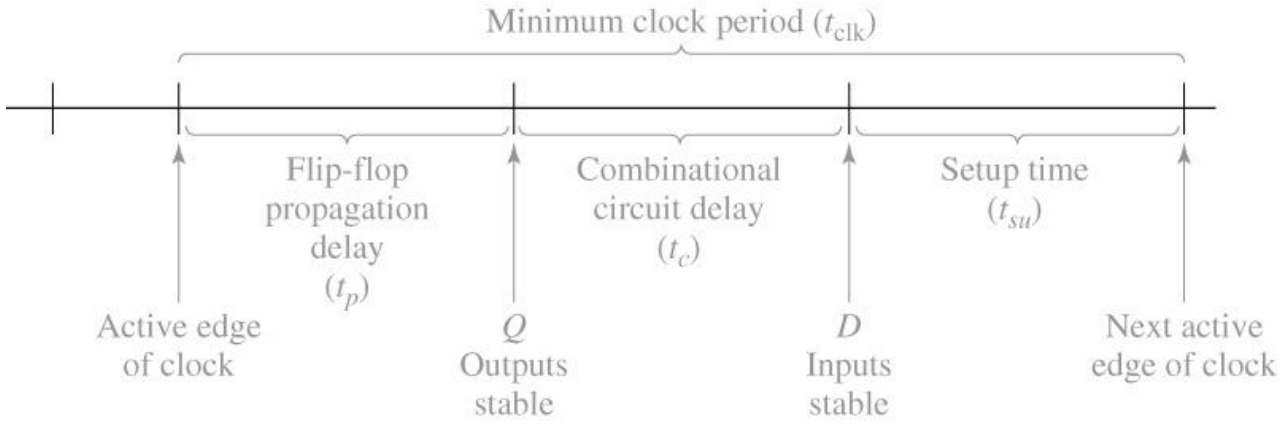
The combinational subcircuit realizes the n output functions and the k next-state function, which serve as inputs to the D flip-flop.

$$
\left.
\begin{aligned}
Z_1 &= f_1(X_1, X_2 \ldots . X_m, Q_1, Q_2, \ldots . Q_k) \\
Z_2 &= f_2(X_1, X_2 \ldots . X_m, Q_1, Q_2, \ldots . Q_k) \\
&\vdots \\
Z_n &= f_n(X_1, X_2, \ldots X_m, Q_1, Q_2, \ldots Q_k)
\end{aligned}
\right\} \text{n output functions}
$$

$$
\left.
\begin{aligned}
Q_1^+ &= D_1 = g_1(X_1, X_2 \ldots . X_m, Q_1, Q_2, \ldots . Q_k) \\
Q_2^+ &= D_2 = g_2(X_1, X_2 \ldots . X_m, Q_1, Q_2, \ldots . Q_k) \\
&\vdots \\
Q_k^+ &= D_k = g_k(X_1, X_2 \ldots . X_m, Q_1, Q_2, \ldots . Q_k)
\end{aligned}
\right\} \text{k next-state functions}
$$

# 13.4 General Models for Sequential Circuit

Figure 13-18: Minimum Clock Period for a Sequential Circuit

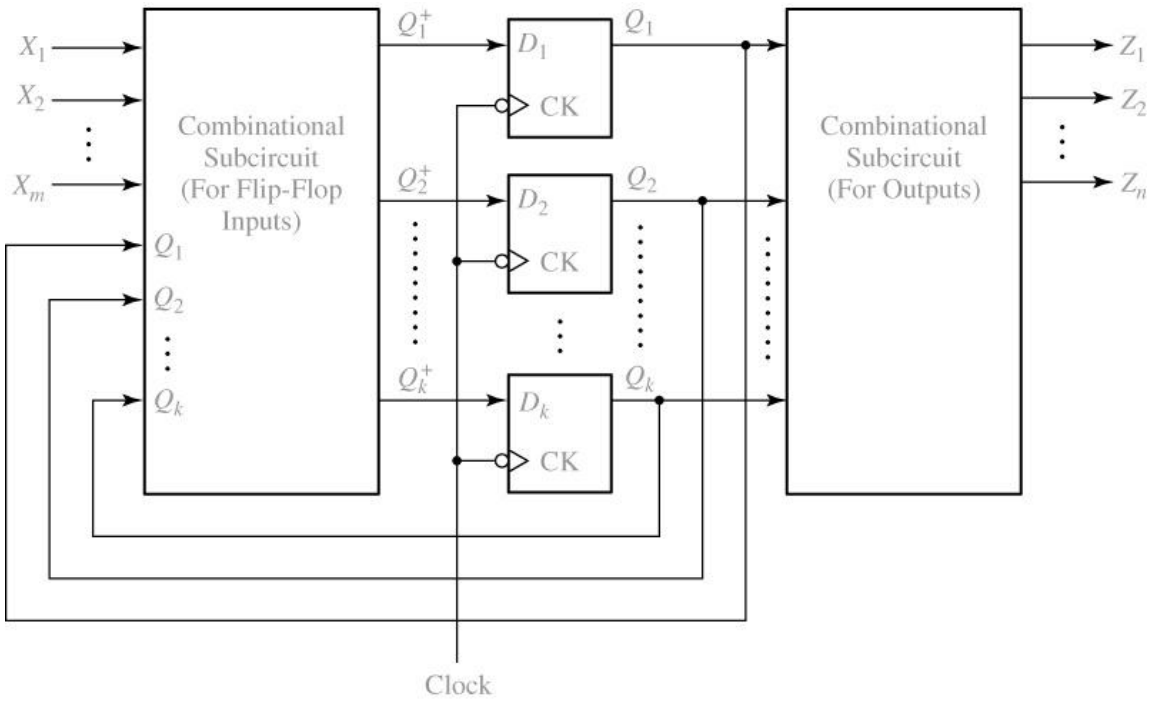



$$t_{clk}(\min) = t_p + t_c + t_{su}$$

$$t_{clk}(\min) = t_x + t_c + t_{su}$$

# 13.4 General Models for Sequential Circuit

Figure 13-19: General Model for Moore Circuit Using Clocked D Flip-Flops



# 13.4 General Models for Sequential Circuit

Table13-5 State Table with Multiple inputs and Outputs

| Present State | Next state X = 0 1 2 3 | Present Output(z) X = 0 1 2 3 |
|---|---|---|
| $S_0$ | $S_3$ $S_2$ $S_1$ $S_0$ | 0 2 3 1 |
| $S_1$ | $S_0$ $S_1$ $S_2$ $S_3$ | 2 2 3 3 |
| $S_2$ | $S_3$ $S_0$ $S_1$ $S_1$ | 0 2 3 1 |
| $S_3$ | $S_2$ $S_2$ $S_1$ $S_0$ | 0 0 1 1 |

$$S^+ = \delta(S, X)$$

$$Z = \lambda(S, X)$$

$$\delta(S_0,1) = S_2 \qquad \delta(S_2,3) = S_1$$

$$\lambda(S_0,1) = 2 \qquad \lambda(S_2,3) = 1$$