CHAPTER 12

REGISTERS AND COUNTERS

Contents

Objectives

1. Explain the operation of registers. Understand how to transfer data between registers using tri-state bus

2. Explain the shift register operation, how to build them and analyze operation. Construct a timing diagram for a shift register

3. Explain the operation of binary counters, how to build them using F/F and gates and analyze operation.

4. Given the present state and desired next state of F/F, determine the required F/F/ inputs

5. Given the desired counting sequence for a counter, derive F/F input equations.

6. Explain the procedures used for deriving F/F input equation.

7. Construct a timing diagram for a counter by tracing signals through the circuit.

12.1 Registers and Register Transfers

Figure 12-1 . 4-Bit D Flip-Flop Registers with Data, Load, Clear, and Clock inputs

Grouped together D F/F

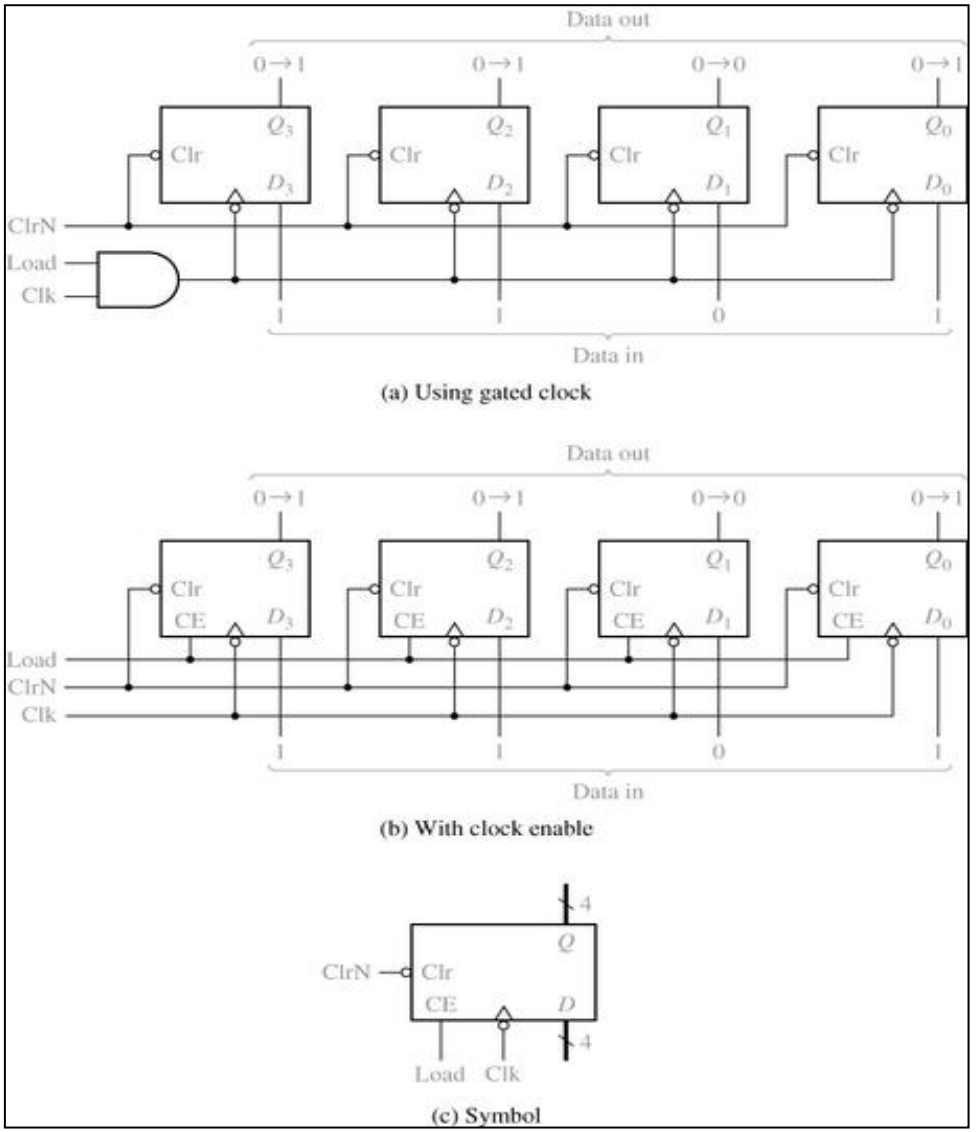
Using gated clock(a)

F/F with clock enable

Figure 12-1(b)

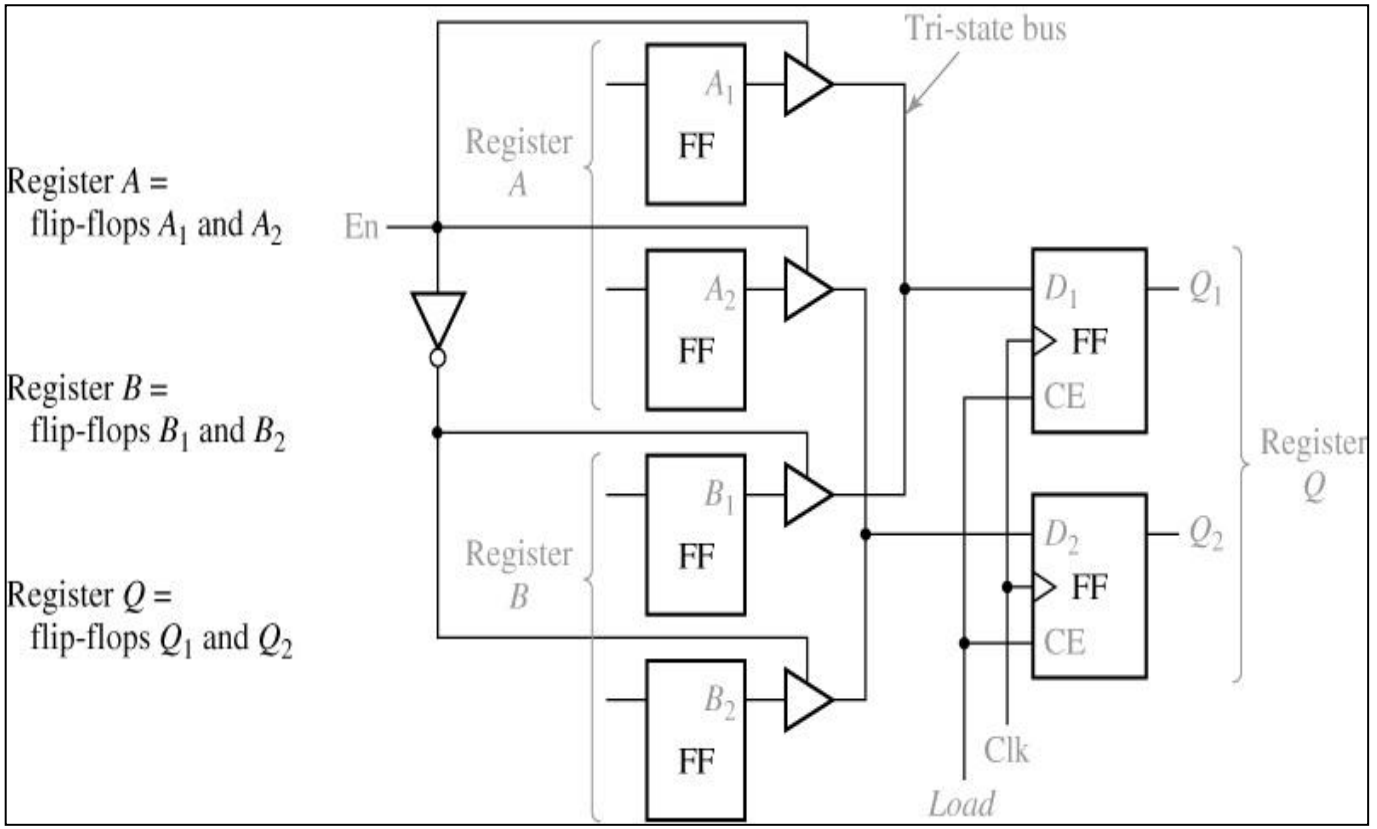
Symbol for the 4-bit register using bus notation

Figure 12-1(c)



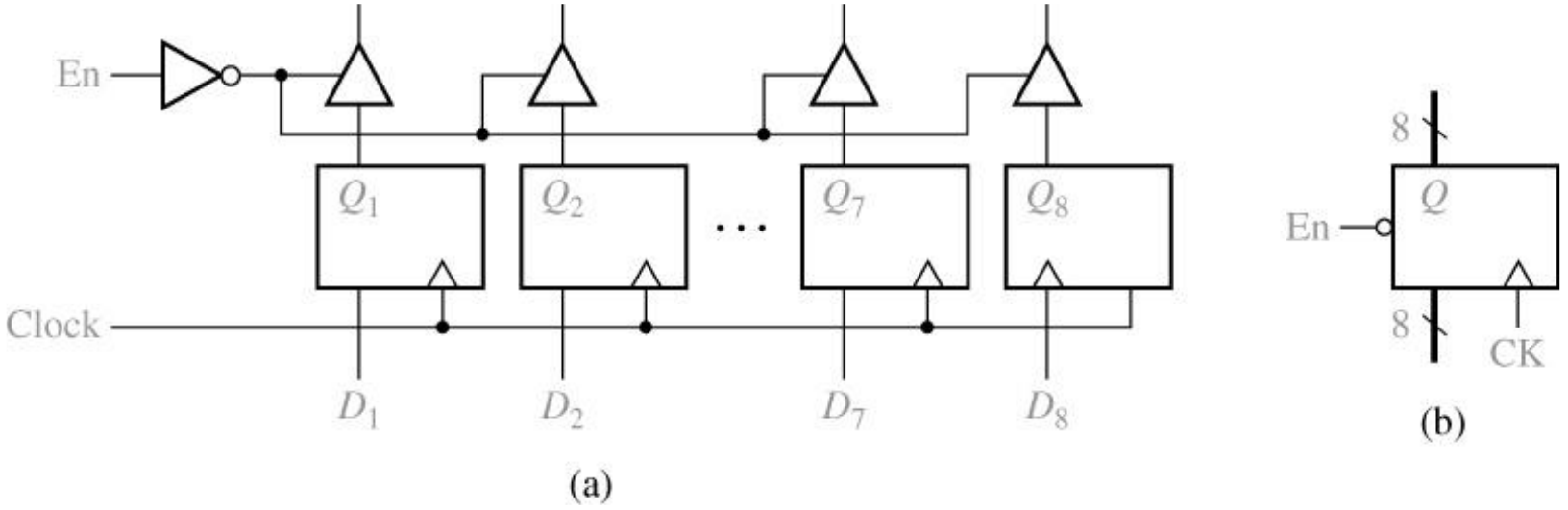
12.1 Registers and Register Transfers

Data Transfer Between Registers



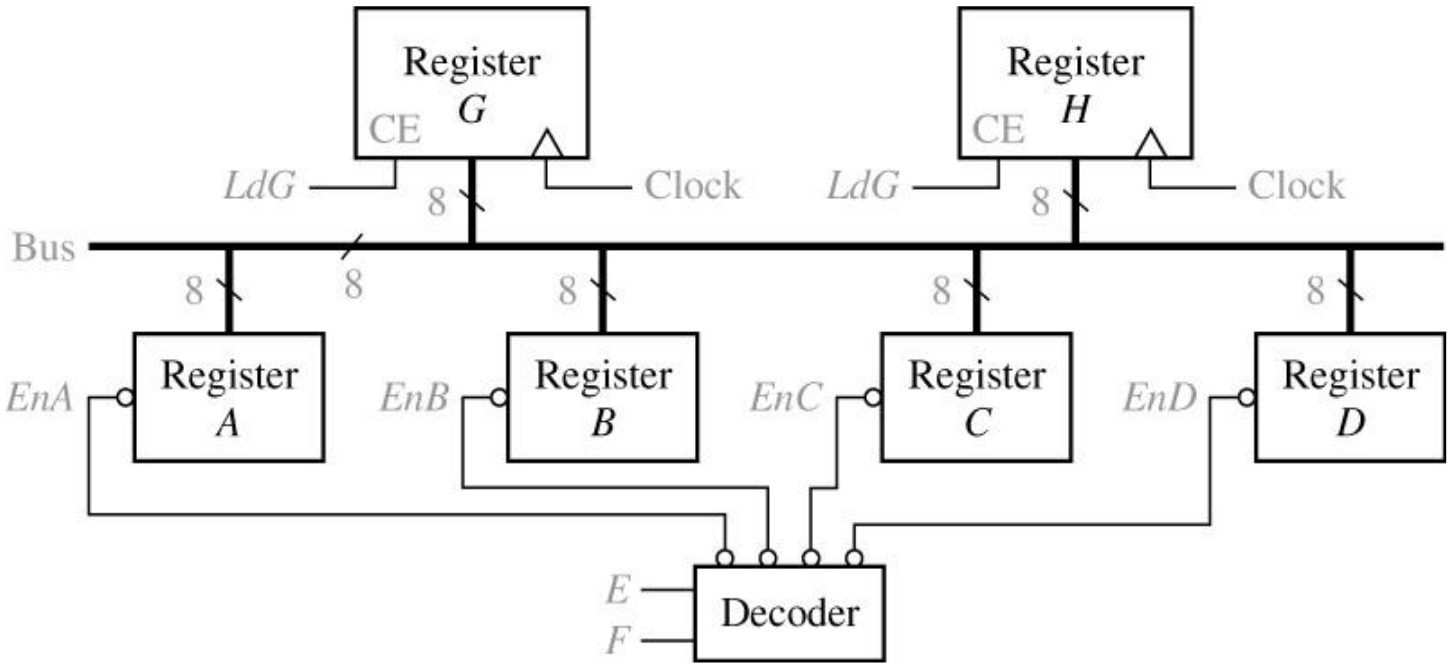
12.1 Registers and Register Transfers

Logic Diagram for 8-Bit Register with Tri-State Output



12.1 Registers and Register Transfers

Data Transfer Using a Tri-State Bus



12.1 Registers and Register Transfers

How data can be transferred?

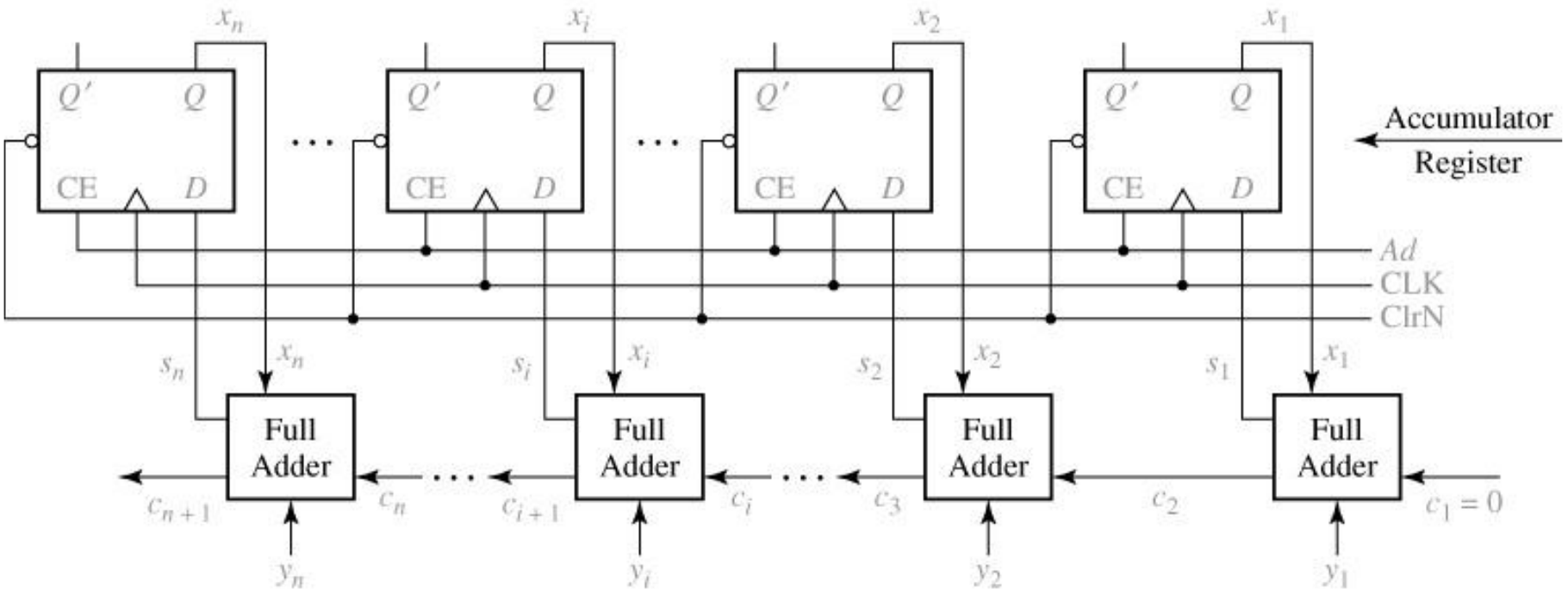
The operation can be summarized as follows:

$$\text{If } EF = 00, A \text{ is stored in } G(\text{or } H).$$
$$\text{If } EF = 01, B \text{ is stored in } G(\text{or } H).$$
$$\text{If } EF = 10, C \text{ is stored in } G(\text{or } H).$$
$$\text{If } EF = 11, D \text{ is stored in } G(\text{or } H).$$

12.1 Registers and Register Transfers

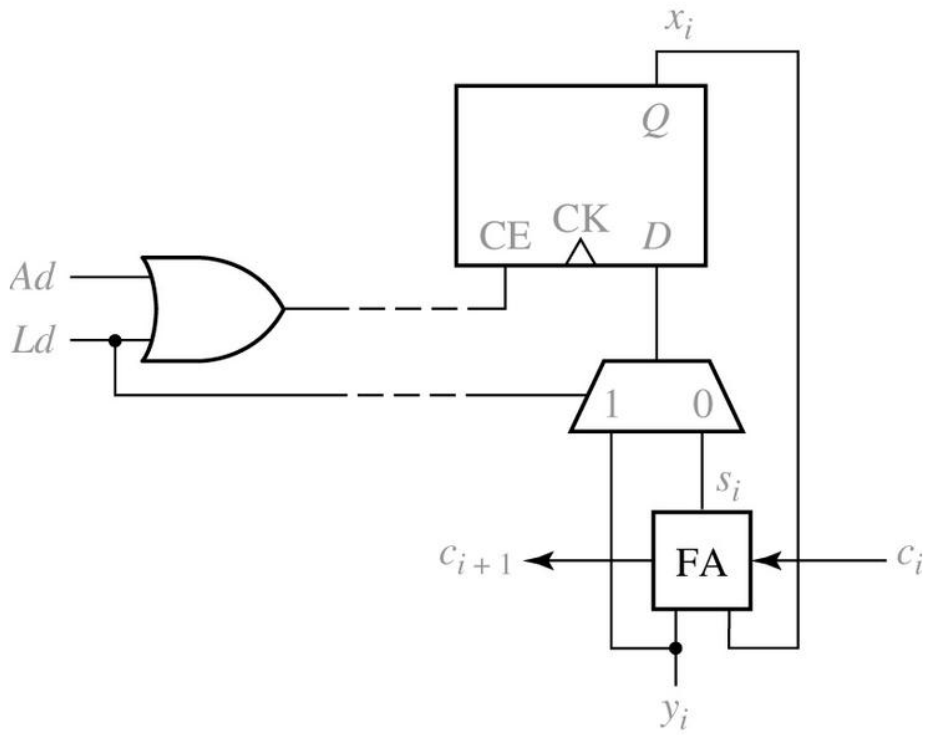
Parallel Adder with Accumulator

N-Bit Parallel Adder with Accumulator



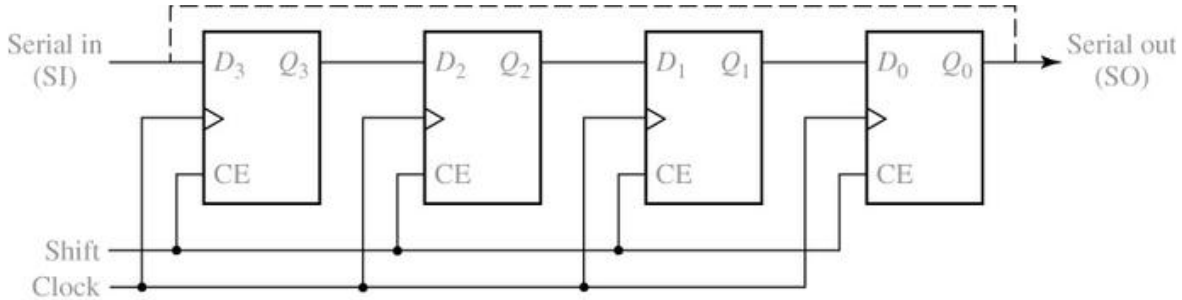
12.1 Registers and Register Transfers

Adder Cell with Multiplexer (Figure 12-6)

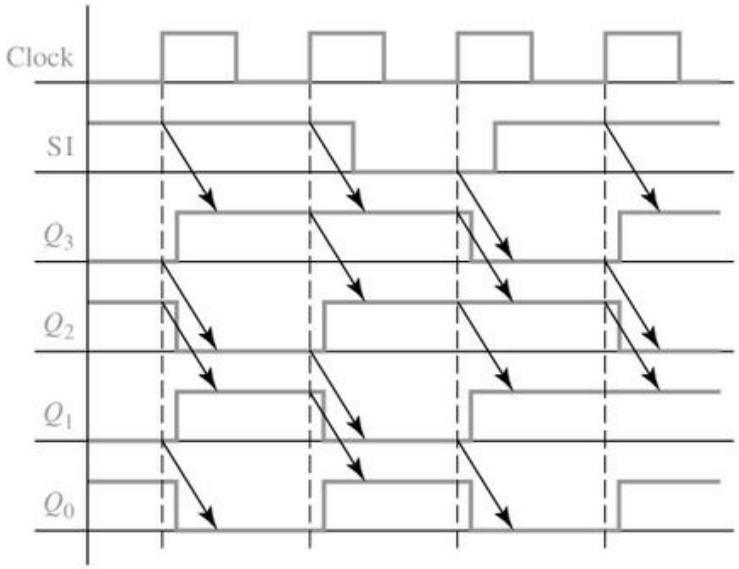


12-2 Shift Registers

Right-Shift Register



(a) Flip-flop connections

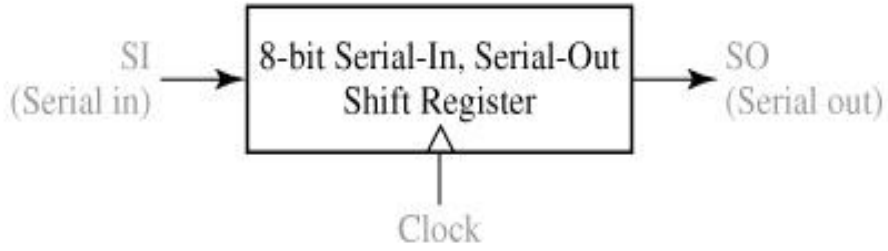


(b) Timing diagram

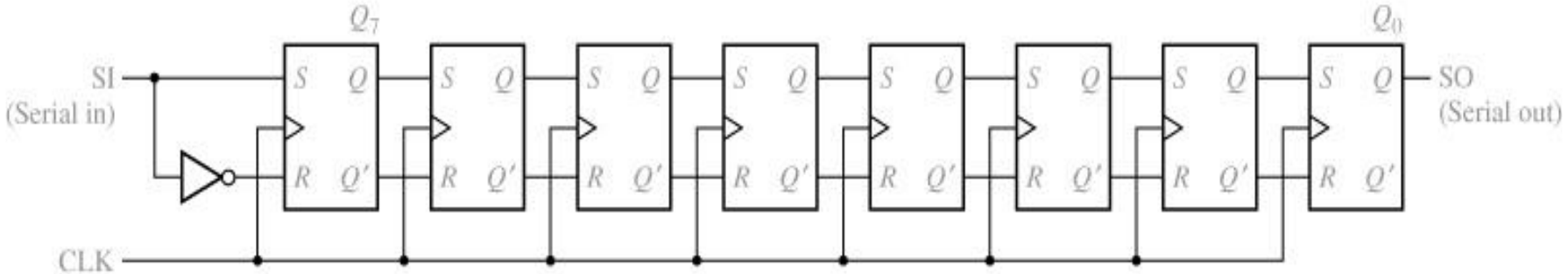
0101→1010→1101→
0110→1011

12-2 Shift Registers

8-Bit Serial-in, Serial-out Shift Register



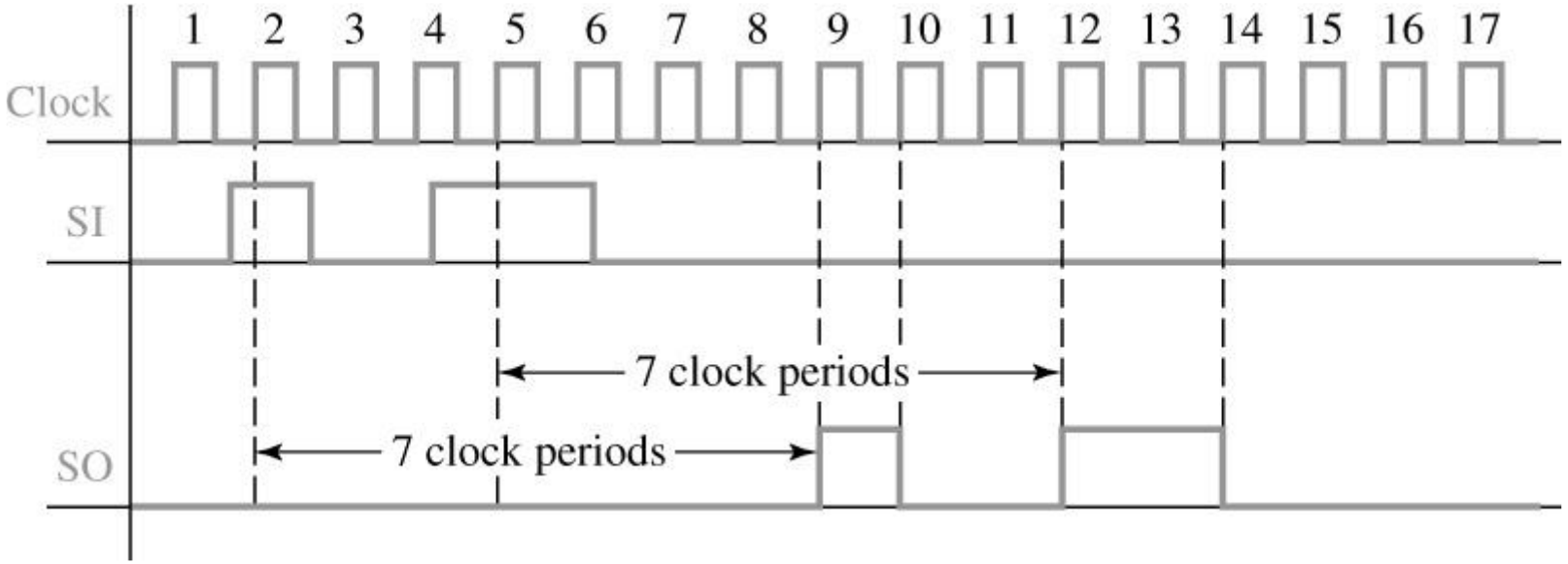
(a) Block diagram



(b) Logic diagram

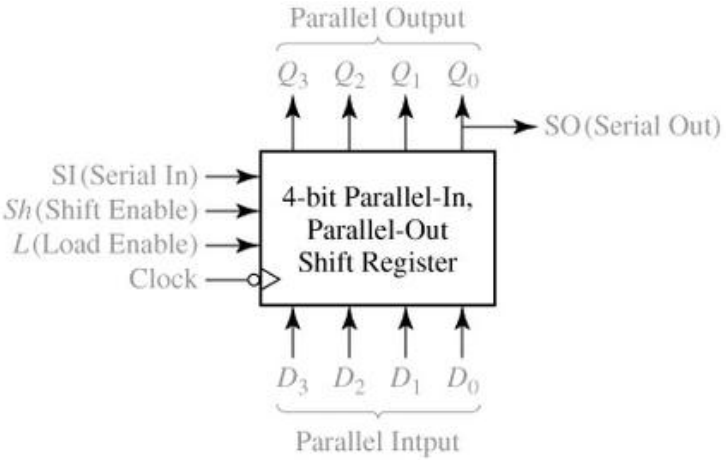
12-2 Shift Registers

Typical Timing Diagram for Shift Register

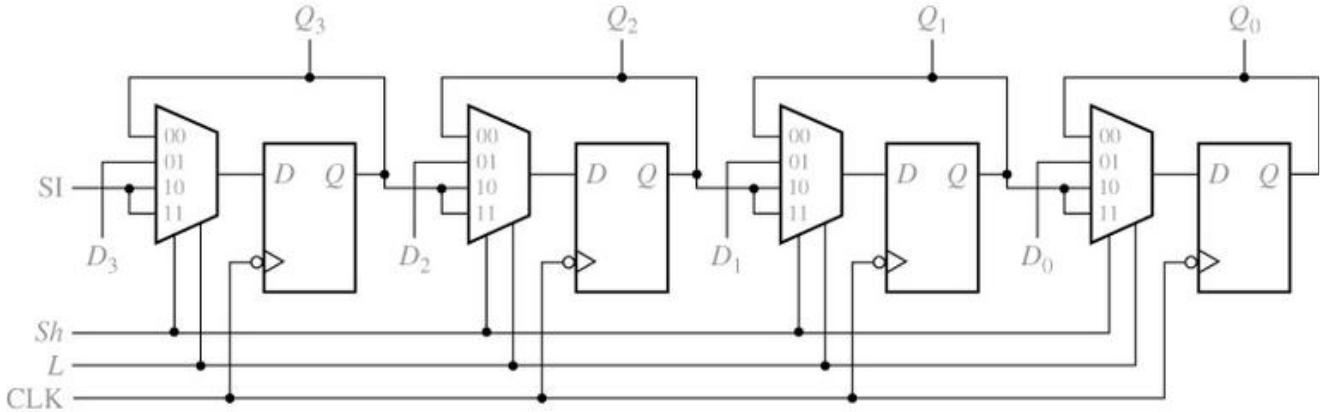


12-2 Shift Registers

Parallel-in, Parallel-Out Right Shift Register



(a) Block diagram



(b) Implementation using flip-flops and MUXes

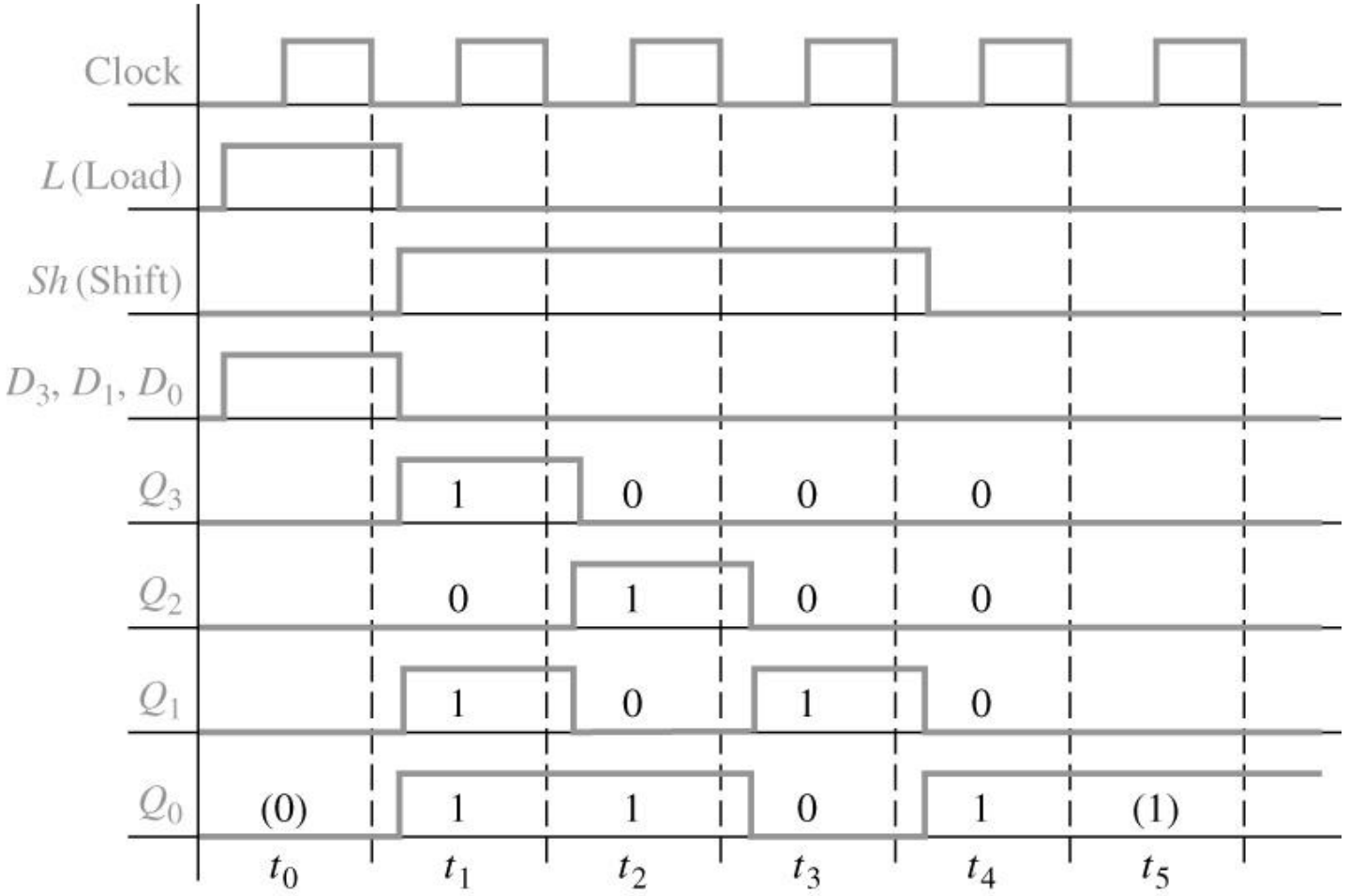
12-2 Shift Registers

Shift Register Operation (Table 12–1)

Inputs		Next State				Action
Sh(Shift)	*L*(Load)	Q_3^+	Q_2^+	Q_1^+	Q_0^+	
0	0	Q_3	Q_2	Q_1	Q_0	no change
0	1	Q_3	Q_2	Q_1	Q_0	load
1	×	SI	Q_3	Q_2	Q_1	right shift

12-2 Shift Registers

Timing Diagram for Shift Register



12-2 Shift Registers

The Next-state equations for the F/F are

$$Q_3^+ = Sh' \cdot L' \cdot Q_3 + Sh' \cdot L \cdot D_3 + Sh \cdot \mathrm{SI}$$

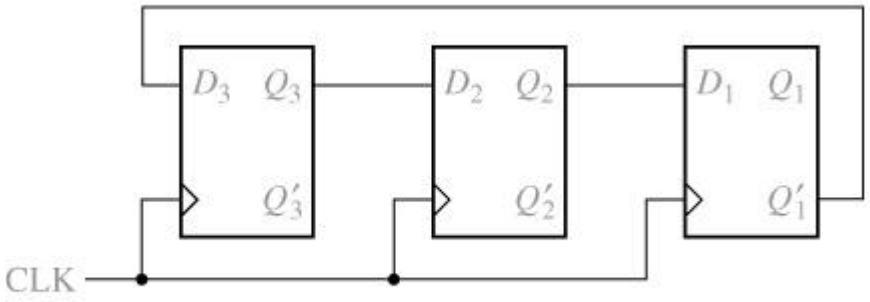
$$Q_2^+ = Sh' \cdot L' \cdot Q_2 + Sh' \cdot L \cdot D_2 + Sh \cdot Q_3$$

$$Q_1^+ = Sh' \cdot L' \cdot Q_1 + Sh' \cdot L \cdot D_1 + Sh \cdot Q_2$$

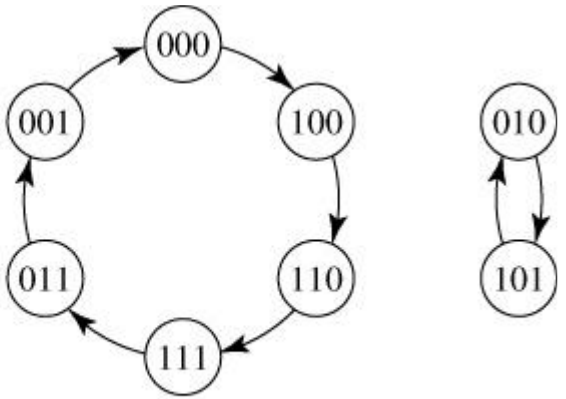
$$Q_0^+ = Sh' \cdot L' \cdot Q_0 + Sh' \cdot L \cdot D_0 + Sh \cdot Q_1$$

12-2 Shift Registers

Shift Register with Inverted Feedback (Figure 12-12) → *Johnson Counter*



(a) Flip-flop connections



(b) State graph

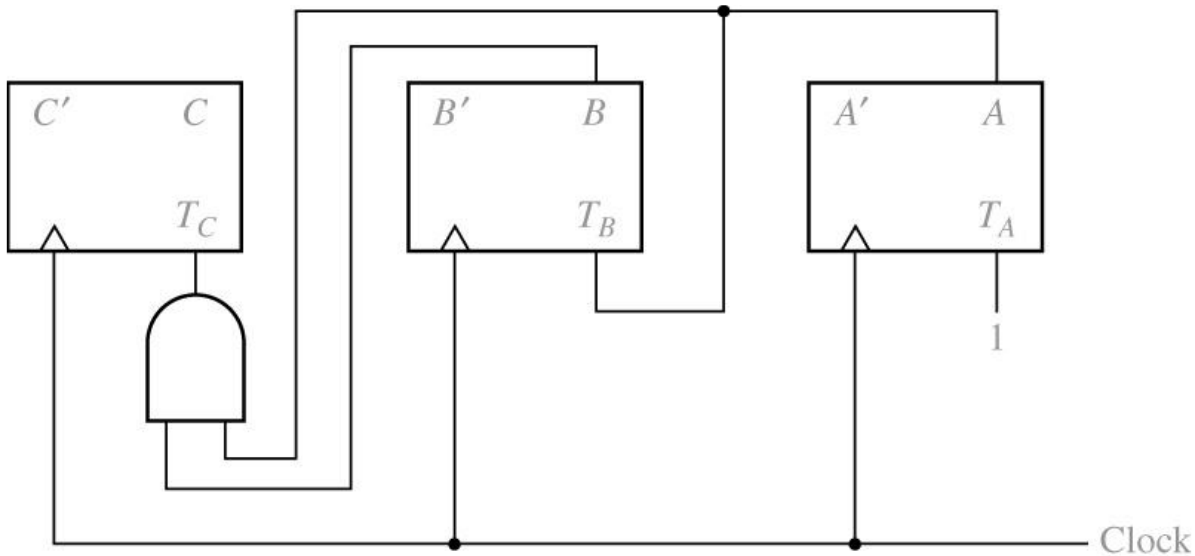
A 3-bit shift register 12-12(a)

Successive states 12-12(b)

12.3 Design of Binary Counters

A binary counter using three T F/F to count clock pulses

Synchronous Binary Counter (Figure 12-13)



Counting sequence

CBA: 000→001→010→011→100→101→110→111→000

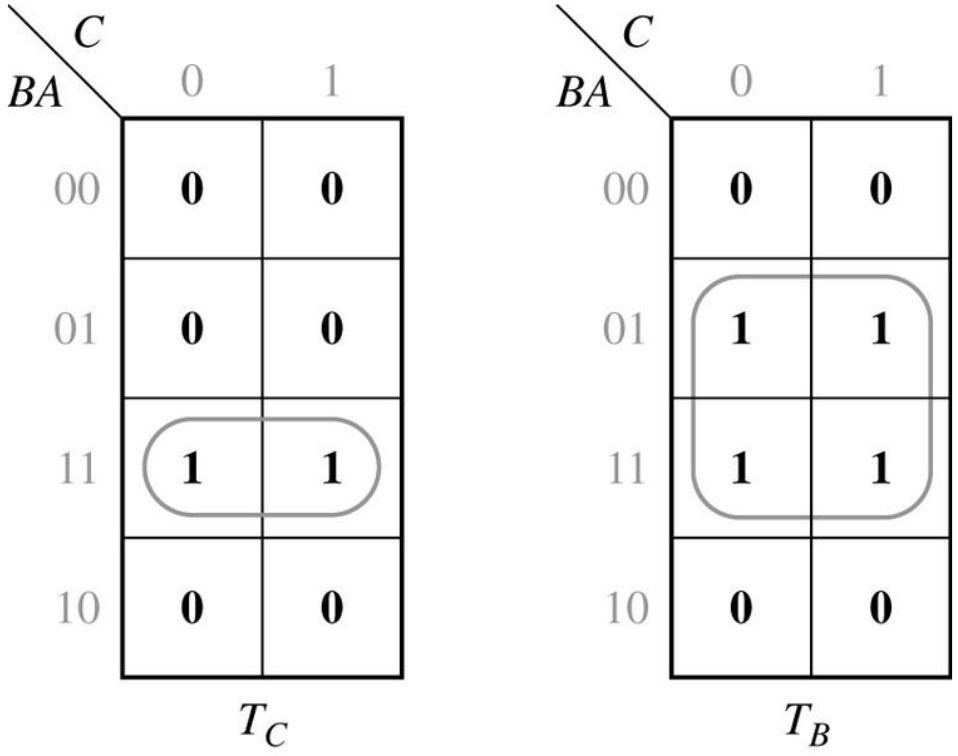
12.3 Design of Binary Counters

State Table for Binary Counter (Table 12–2)

Present State			Next State			Flip - Flop Inputs		
C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

12.3 Design of Binary Counters

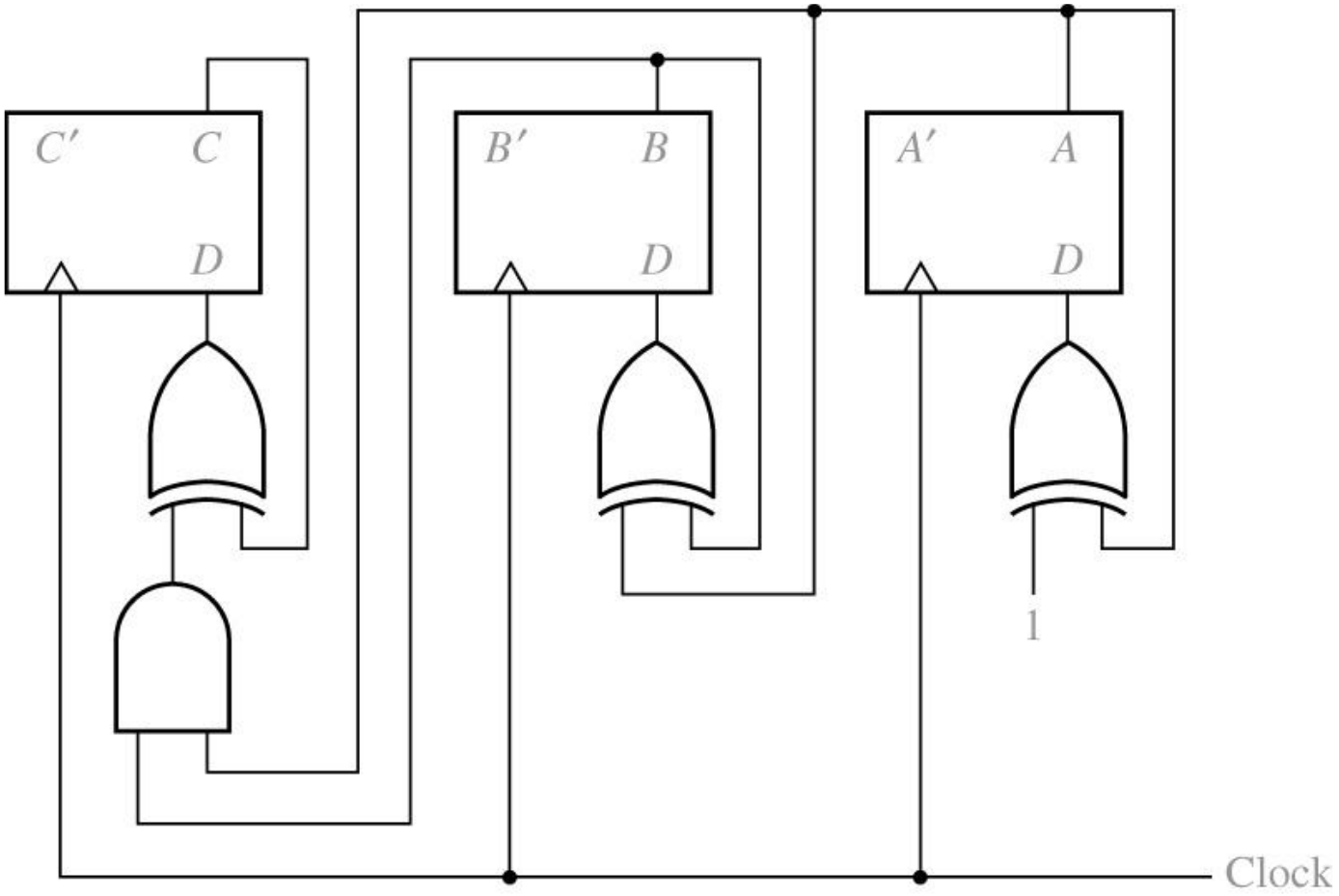
Karnaugh Map for Binary Counter (Figure 12-14)



$$T_a = 1, \quad T_b = A, \quad T_c = AB$$

12.3 Design of Binary Counters

Binary Counter with D Flip-Flops (Figure 12-15)

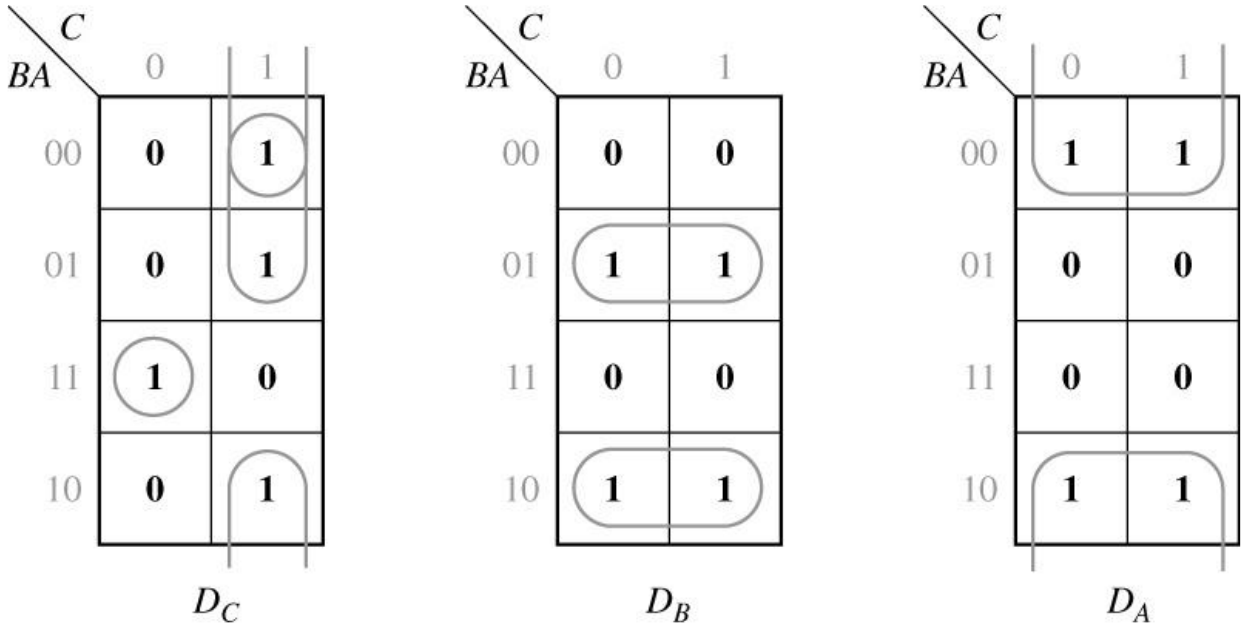


12.3 Design of Binary Counters

The D input equations derived from the maps are

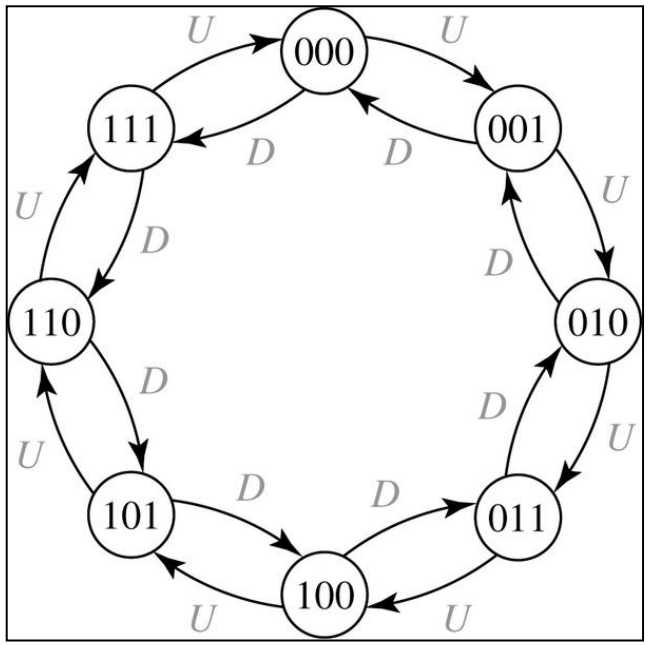
$$D_A = A^+ = A'$$
$$D_B = B^+ = BA' + B'A = B \oplus A$$
$$D_C = C^+ = C'BA + CB' + CA' = C'BA + C(BA)' = C \oplus BA$$

Karnaugh Maps for D Flip-Flops (Figure 12-16)



12.3 Design of Binary Counters

State Graph and Table for Up-Down counter (Figure 12-17)



CBA	$C^+B^+A^+$	
	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

When U=1, Up counting

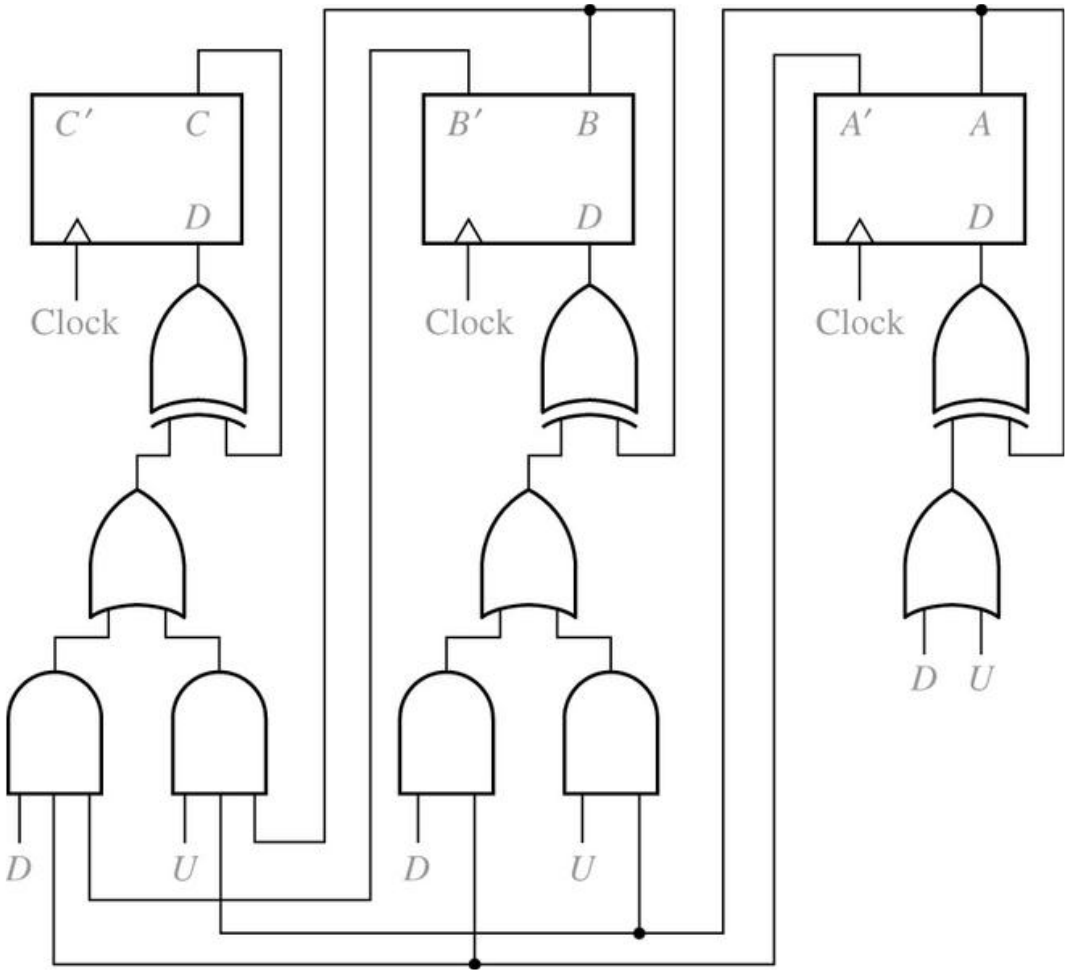
When D=1, Down counting

12.3 Design of Binary Counters

The up-down counter can be implemented using D F/F and gate

Binary Up-Down Counter

(Figure 12-18)



12.3 Design of Binary Counters

The corresponding logic equations are

$$D_A = A^+ = A \oplus (U + D)$$
$$D_B = B^+ = B \oplus (UA + DA')$$
$$D_C = C^+ = C \oplus (UBA + DB'A')$$

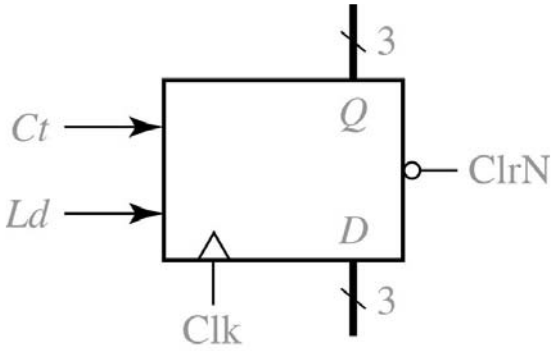
When U=0 and D=1, these equations reduce to

$$D_A = A^+ = A \oplus 1 = A' \quad (A \text{ change state every clock cycle})$$
$$D_B = B^+ = B \oplus A' \quad (B \text{ change state when } A = 0)$$
$$D_C = C^+ = C \oplus B'A' \quad (C \text{ change state when } B = A = 0)$$

12.3 Design of Binary Counters

Loadable Counter with Count Enable (Figure 12-19)

Loadable counter (Figure 12-19(a))



(a)

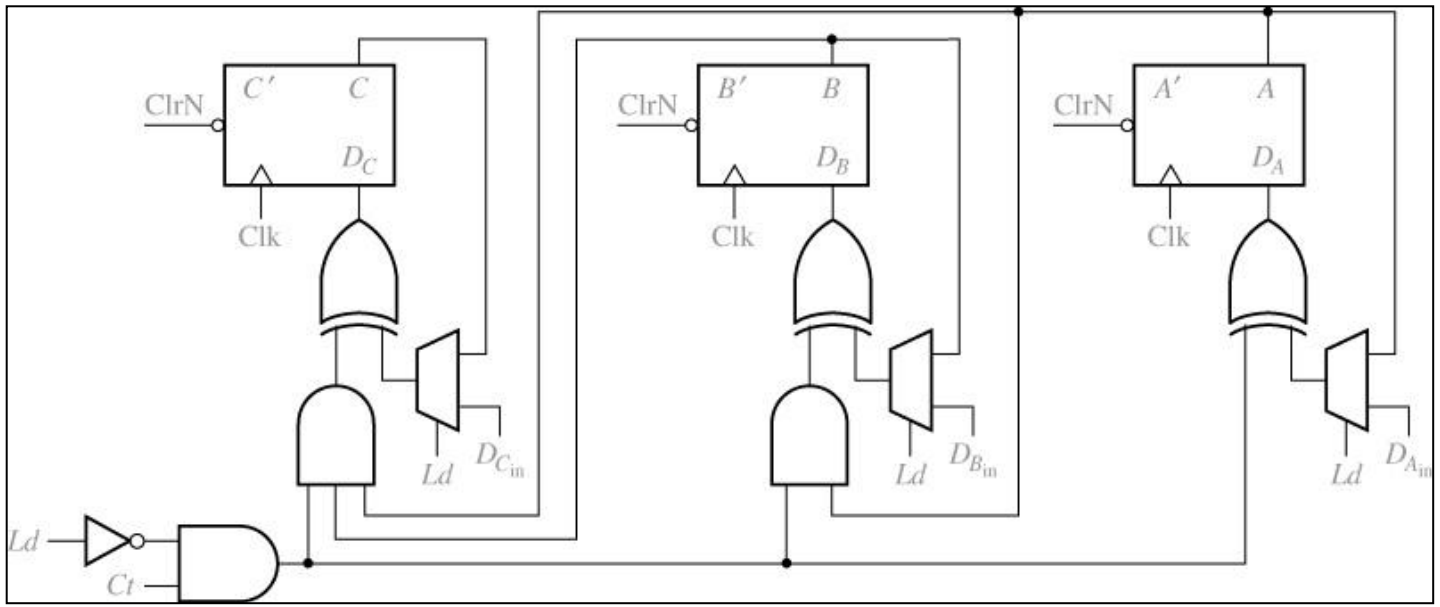
Summarizes the counter operation (Figure 12-19(b))

$ClrN$	Ld	Ct	C^+	B^+	A^+	
0	×	×	0	0	0	
1	1	×	D_C	D_B	D_A	(*load*)
1	0	0	C	B	A	(*no change*)
1	0	1	present state +1			

(b)

12.3 Design of Binary Counters

Circuit for Figure 12-19 (Figure 12-20)



12.3 Design of Binary Counters

The next-state equations for the counter of Figure 12-20

$$A^{+} = D_A = (Ld' \cdot A + Ld \cdot D_{Ain}) \oplus Ld' \cdot Ct$$

$$B^{+} = D_B = (Ld' \cdot B + Ld \cdot D_{Bin}) \oplus Ld' \cdot Ct \cdot A$$

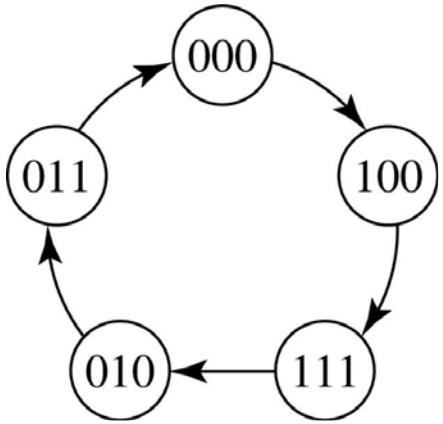
$$C^{+} = D_c = (Ld' \cdot C + Ld \cdot D_{Cin}) \oplus Ld' \cdot Ct \cdot B \cdot A$$

12.4 Counters for Other Sequences

The sequence of states of a counter is not in straight binary order.

State Graph for Counter

(Figure 12-21)



State Table for Figure 21.21

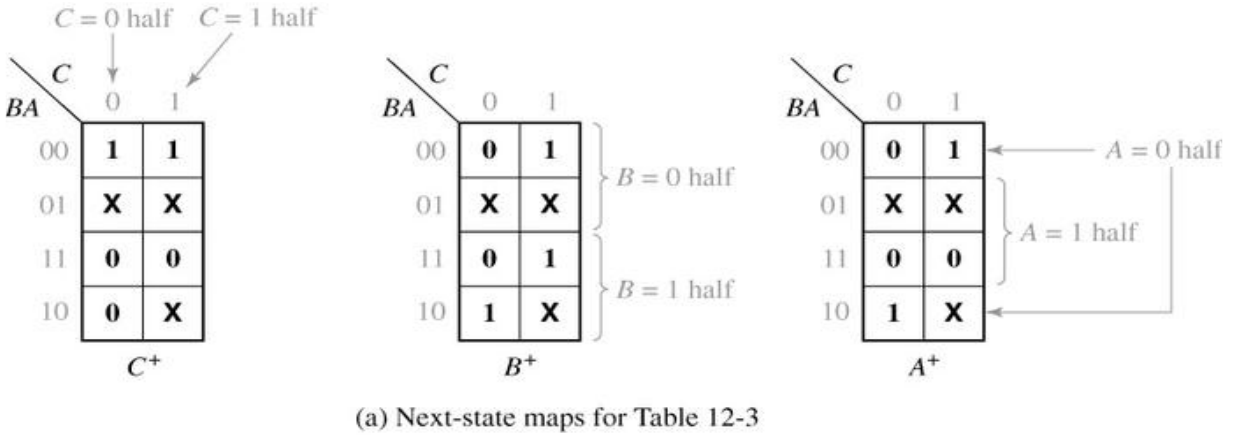
(Table 12-3)

C	B	A	C^+	B^+	A^+
0	0	0	1	0	0
0	0	1	-	-	-
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	-	-	-
1	1	0	-	-	-
1	1	1	0	1	0

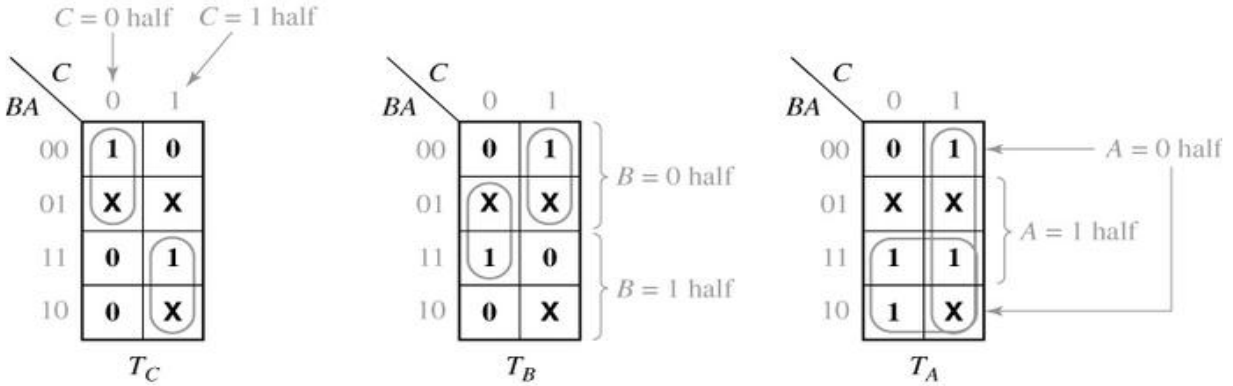
12.4 Counters for Other Sequences

The next-state maps in Figure 12-22(a) are easily plotted from inspection of Table 12-3 → Use T-F/F

Figure 12-22



(a) Next-state maps for Table 12-3



(b) Derivation of T inputs

12.4 Counters for Other Sequences

Input for T Flip-Flop

(Table 12-4)

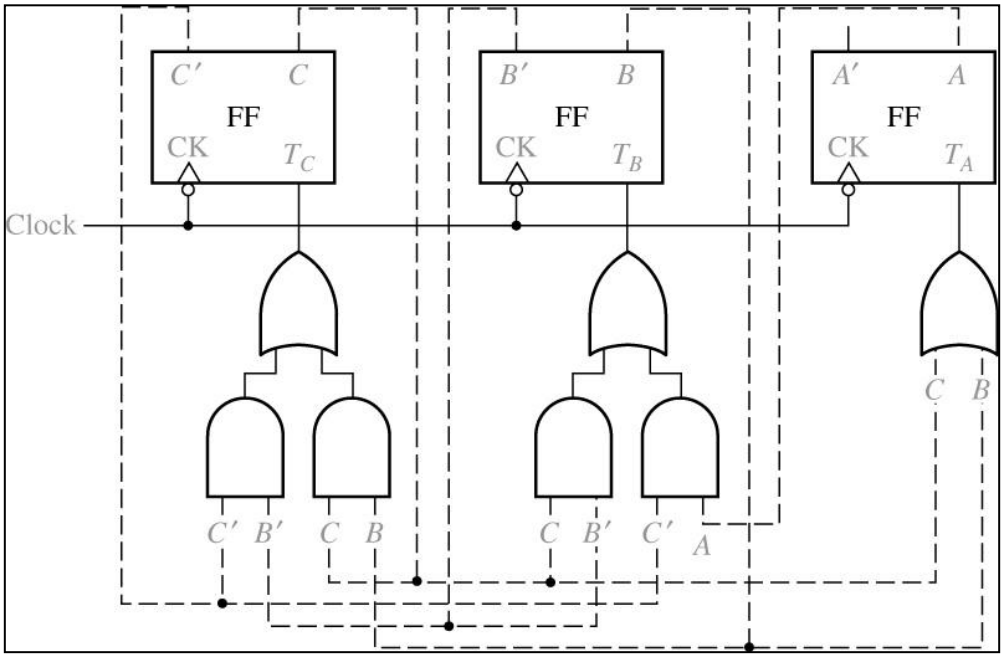
Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

$$T = Q^+ \oplus Q$$

Counter Using

T Flip-Flops

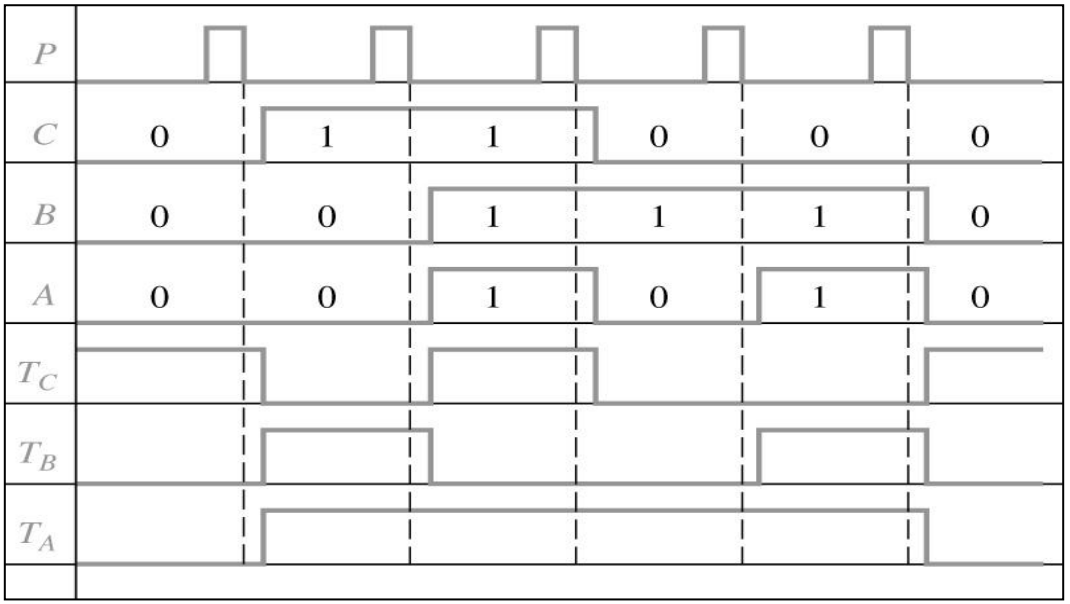
(Figure 12-23)



12.4 Counters for Other Sequences

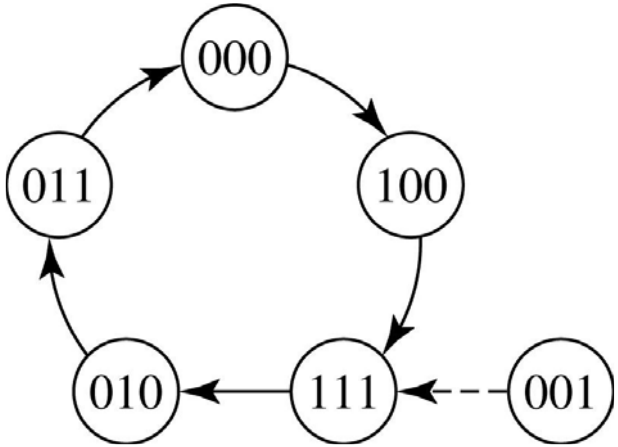
Timing Diagram for Figure 12-23

(Figure 12-24)



State Graph for Counter

(Figure 12-25)



12.4 Counters for Other Sequences

Summary:

1.Form a state table which gives the next F/F states for each combination of present F/F states.

2.Plot the next-state maps from the table.

3.Plot a T input map for each F/F .

4.Find the T input equations from the maps and realize the circuit.

12.4 Counters for Other Sequences

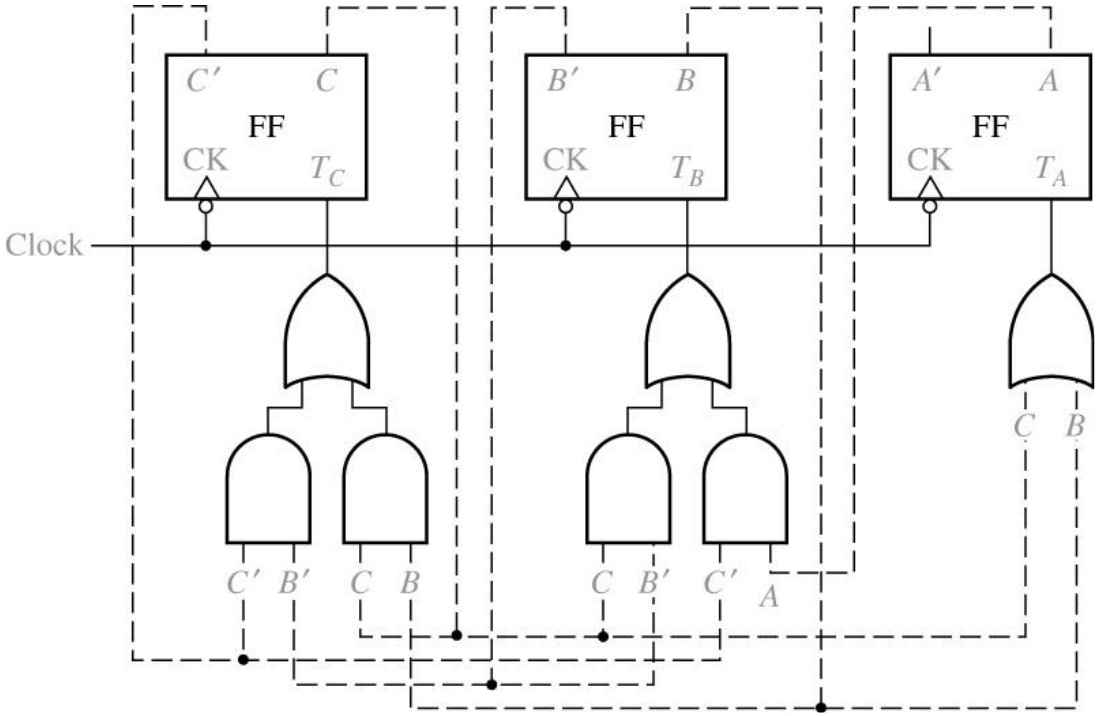
Counter Design Using D Flip-Flop

Following equations can be read from Figure 12-22(a):

$$D_C = C^+ = B' \qquad D_B = B^+ = C + BA'$$

$$D_A = A^+ = CA' + BA' = A'(C + B)$$

Counter of Figure 12-21 Using D Flip-Flops (Figure 12-26)



12.5 Counter Design Using S-R and J-K Flip-Flops

S-R Flip-Flop Inputs (Table 12-5)

S	R	Q	Q^+	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	-	Inputs not allowed
1	1	1	-	

(a)

Q	Q^+	R	S
0	0	0	0
		0	1
0	1	1	0
1	0	0	1
1	1	0	0
		1	0

(b)

Q	Q^+	R	S
0	0	0	×
0	1	1	0
1	0	0	1
1	1	×	0

(c)

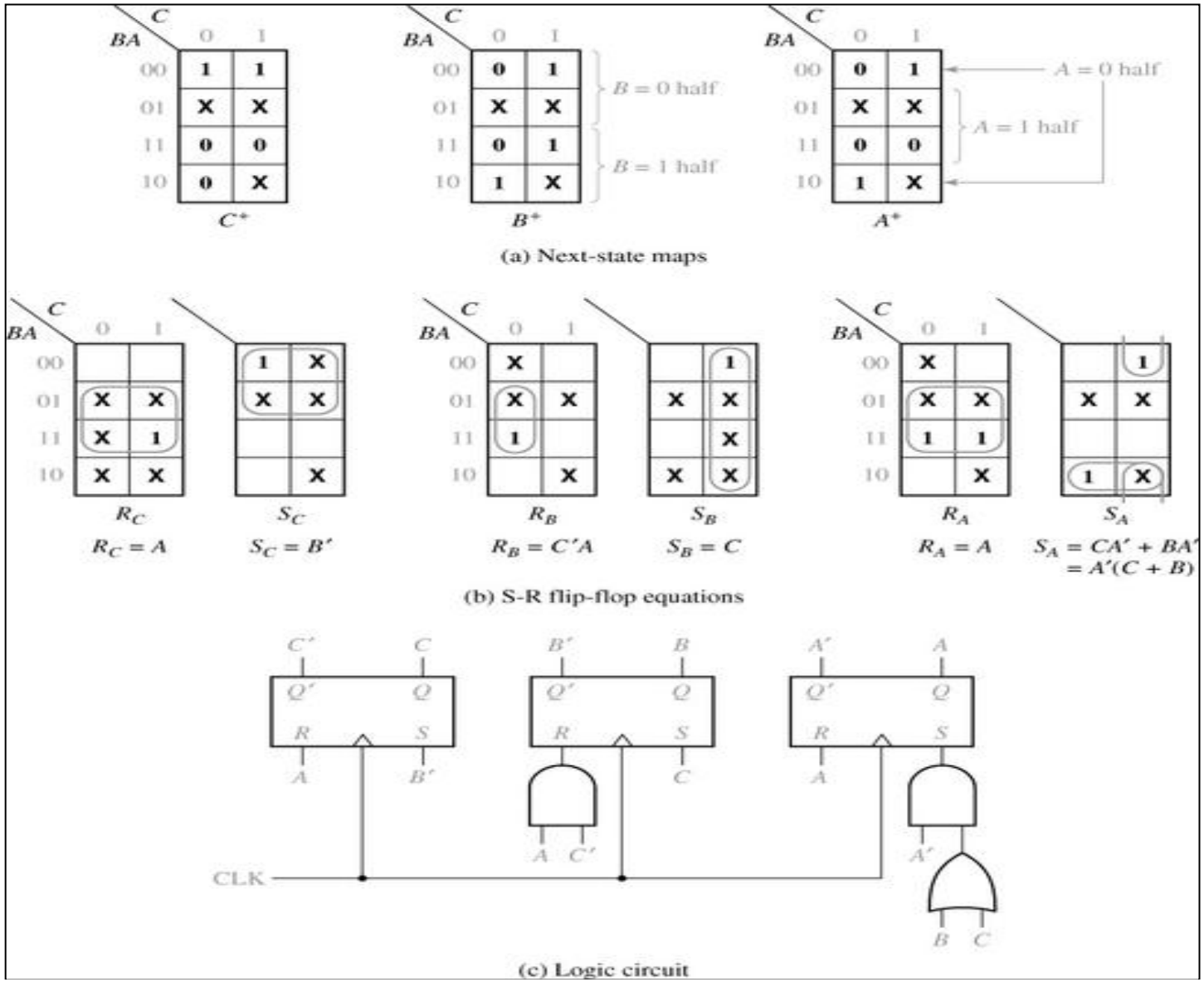
12.5 Counter Design Using S-R and J-K Flip-Flops

With columns added for the S and R flip-flop inputs (Table 12-6)

C	B	A	C^+	B^+	A^+	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	1	0	0	1	0	0	×	0	×
0	0	1	-	-	-	×	×	×	×	×	×
0	1	0	0	1	1	0	×	×	0	1	0
0	1	1	0	0	0	0	×	0	1	0	1
1	0	0	1	1	1	×	0	1	0	1	0
1	0	1	-	-	-	×	×	×	×	×	×
1	1	0	-	-	-	×	×	×	×	×	×
1	1	1	0	1	0	0	1	×	0	0	1

12.5 Counter Design Using S-R and J-K Flip-Flops

Counter Design Using S-R Flip-Flop



12.5 Counter Design Using S-R and J-K Flip-Flops

J-K Flip-Flop Inputs (Table 12-7)

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(a)

Q	Q^+	J	K
0	0	0	0
		0	1
0	1	1	0
		1	1
1	0	0	1
		1	1
1	1	0	0
		1	0

(b)

Q	Q^+	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

(c)

12.5 Counter Design Using S-R and J-K Flip-Flops

With columns added for the J and K flip-flop inputs (Table 12-8)

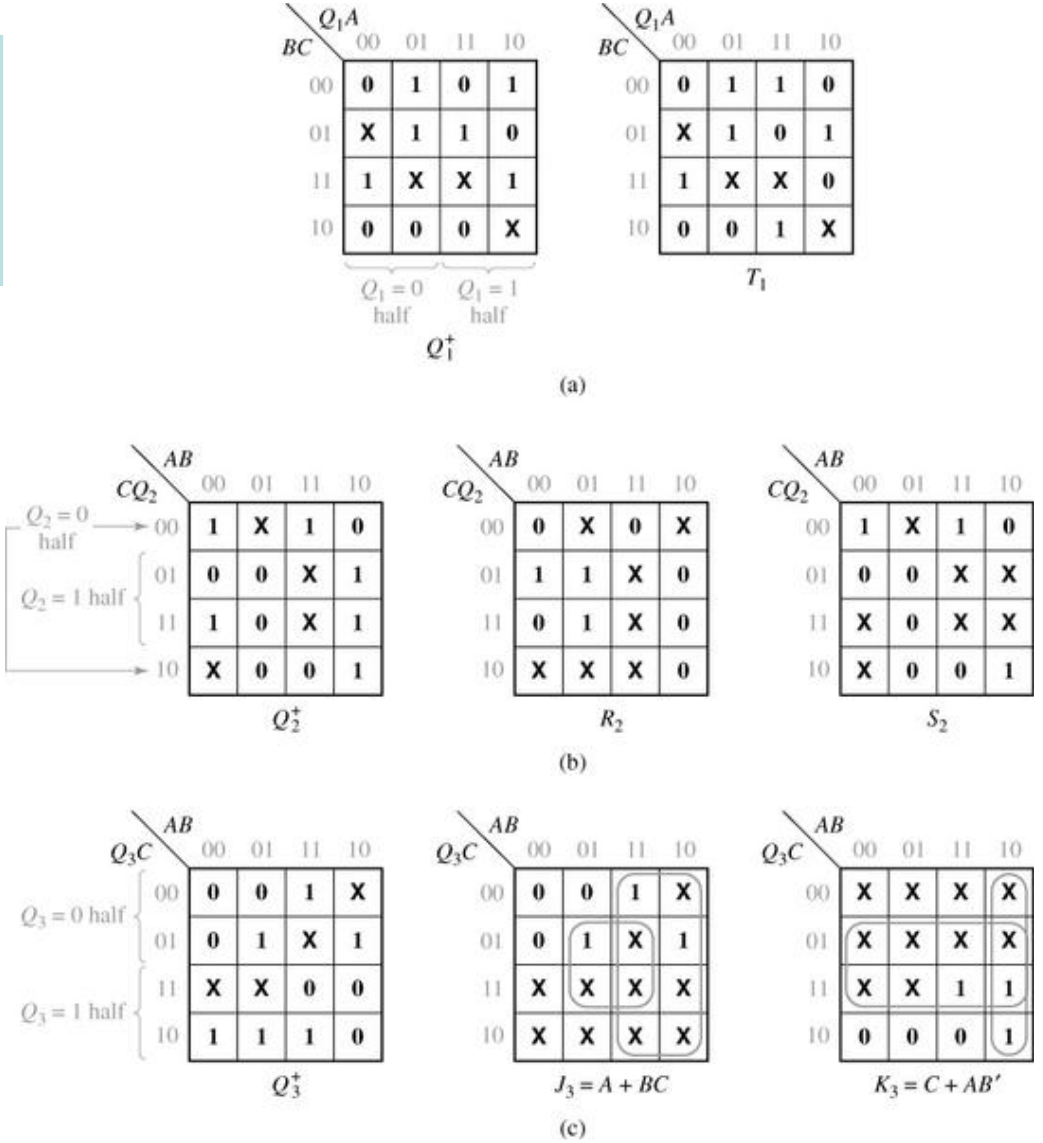
C	B	A	C^+	B^+	A^+	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	1	0	0	1	×	0	×	0	×
0	0	1	-	-	-	×	×	×	×	×	×
0	1	0	0	1	1	0	×	×	0	1	×
0	1	1	0	0	0	0	×	×	1	×	1
1	0	0	1	1	1	×	0	1	×	1	×
1	0	1	-	-	-	×	×	×	×	×	×
1	1	0	-	-	-	×	×	×	×	×	×
1	1	1	0	1	0	×	1	×	0	×	1

12.6 Derivation of Flip-Flop Input Equations-Summary

Counter of Figure 12-21

Using J-K Flip-Flops

(Figure 12-28)



12.6 Derivation of Flip-Flop Input Equations-Summary

Determination of Flip-Flop Input Equations from Next-State Equations Using Karnaugh Maps (Table 12-9)

Type of Flip-Flop	Input	$Q = 0$		$Q = 1$		Rules for Forming Input Map From Next-State Map*	
		$Q^+ = 0$	$Q^+ = 1$	$Q^+ = 0$	$Q^+ = 1$	$Q = 0$ Half of Map	$Q = 1$ Half of Map
Delay	D	0	1	0	1	no change	no change
Trigger	T	0	1	1	0	no change	complement
Set-Reset	S	0	1	0	X	no change	replace 1's with X's**
	R	X	0	1	0	replace 0's with X's**	complement
J-K	J	0	1	X	X	no change	fill in with X's
	K	X	X	1	0	fill in with X's	complement

Q^+ means the next state of Q

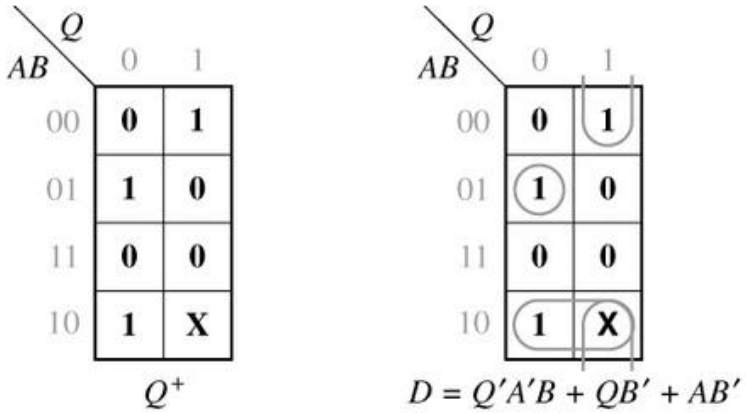
X is a don't care

*Always copy X's from the next-state map onto the input maps first.

**Fill in the remaining squares with 0's.

12.6 Derivation of Flip-Flop Input Equations-Summary

Example (illustrating the use of Table 12-9)



AB \ Q	0	1
00	0	1
01	1	0
11	0	0
10	1	X

Q^+

Next-state map

AB \ Q	0	1
00	0	1
01	1	0
11	0	0
10	1	X

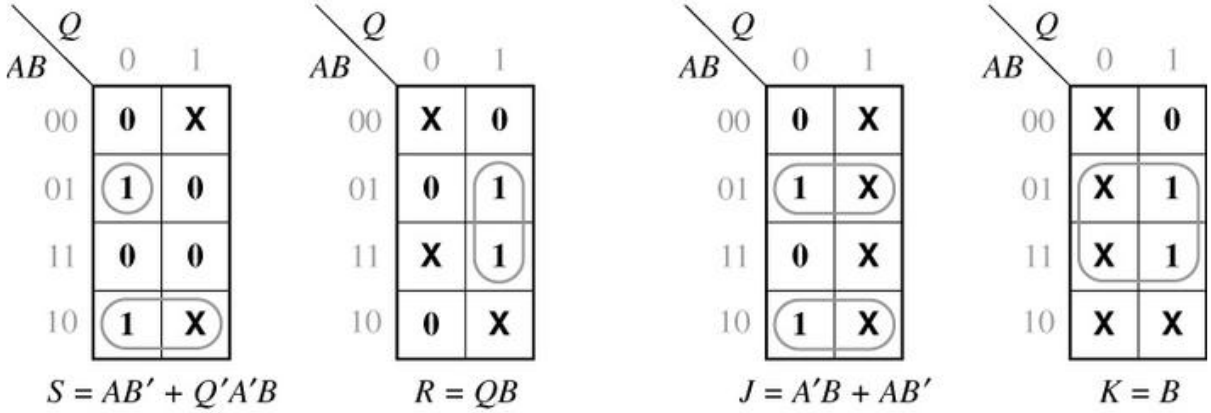
$D = Q'A'B + QB' + AB'$

D input map

AB \ Q	0	1
00	0	0
01	1	1
11	0	1
10	1	X

$T = A'B + AB' + QB$

T input map



AB \ Q	0	1
00	0	X
01	1	0
11	0	0
10	1	X

$S = AB' + Q'A'B$

AB \ Q	0	1
00	X	0
01	0	1
11	X	1
10	0	X

$R = QB$

S-R input maps

AB \ Q	0	1
00	0	X
01	1	X
11	0	X
10	1	X

$J = A'B + AB'$

AB \ Q	0	1
00	X	0
01	X	1
11	X	1
10	X	X

$K = B$

J-K input maps

12.6 Derivation of Flip-Flop Input Equations-Summary

Derivation of Flip-Flop Input Equations Using 4-Variable Maps (Figure 12-29)