CHAPTER 11

LATCHES AND FLIP-FLOPS

Contents

Objectives

1. Explain in words the operation of S-R and gated D latches

2. Explain in words the operation of D, D-CE, S-R, J-K and T flip-flops

3. Make a table and derive the characteristic (next-state) equation for such latches and flip-flops. State any necessary restrictions on the input signals

4. Draw a timing diagram relating the input and output of such latches flip-flops

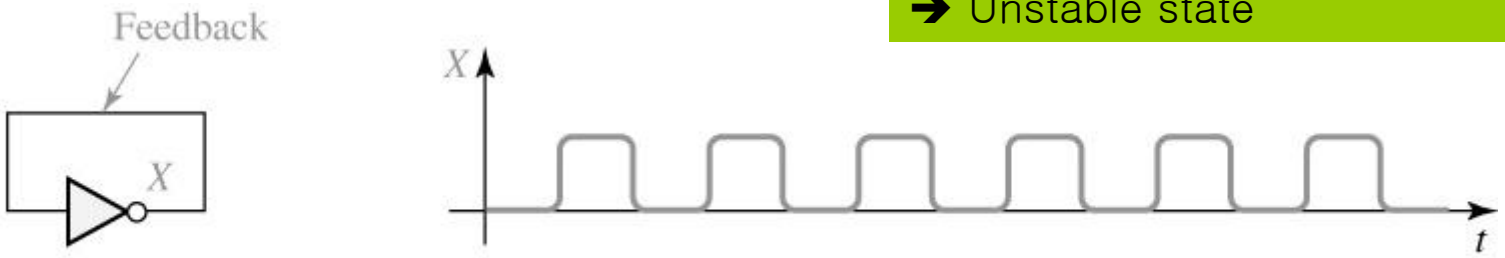
5. Show how latches and flip-flops can be constructed using gates. Analyze the operation of a flip-flop that is constructed of gates and latches

11.1 Introduction

To construct a switching circuit has a memory, must introduce *feedback* to circuit

Fig 11-1.

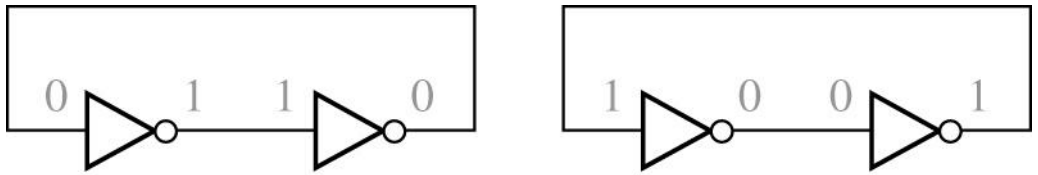
➔ Unstable state



(a) Inverter with feedback (b) Oscillation at inverter output

Fig 11-2.

➔ Stable state



(a) (b)

11.2 Set-Reset Latch

Fig 11-3. S=R=0 (Q=0) → S=1, R=0

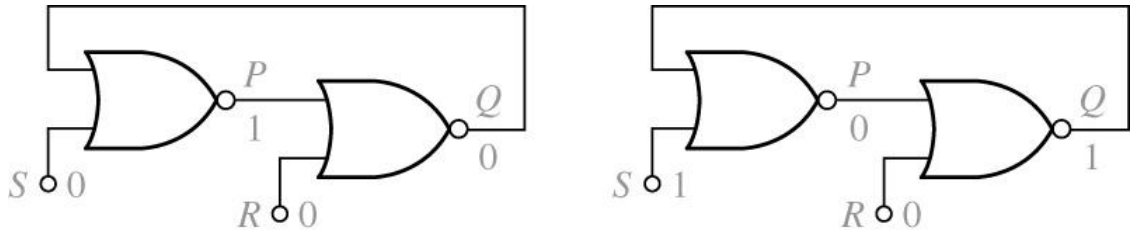
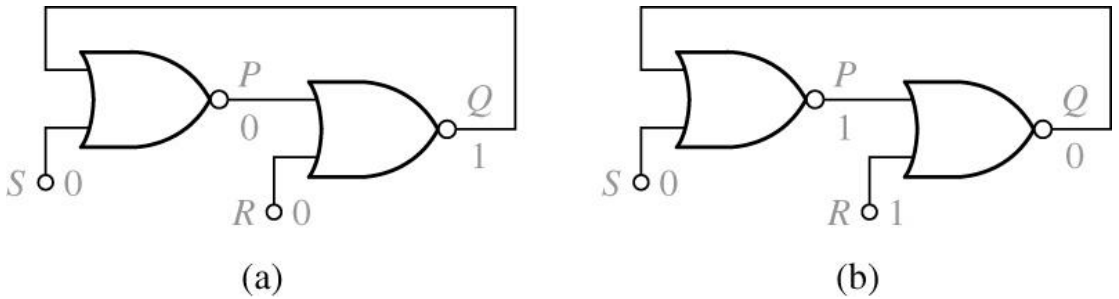


Fig 11-4. S=R=0 (Q=1)→ S=0, R=1



11.2 Set-Reset Latch

Fig 11-5. S-R Latch(cross-coupled structure)

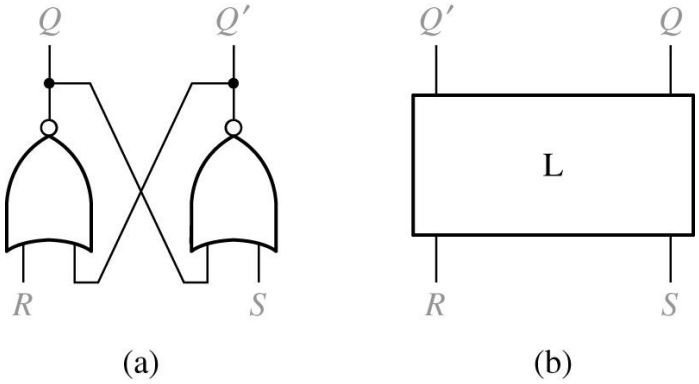
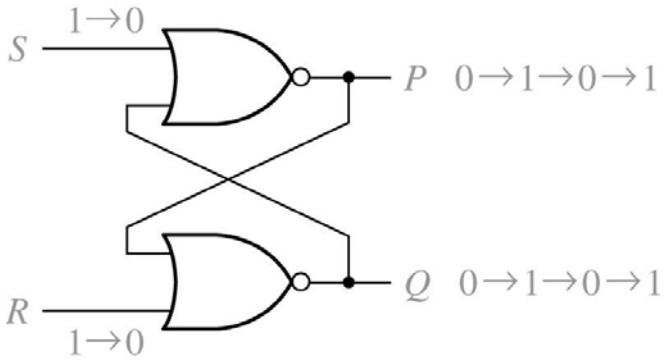


Fig 11-6. Improper S-R Latch Operation (S=R=1; prohibited)



11.2 Set-Reset Latch

Fig 11-7. Timing Diagram for S-R Latch

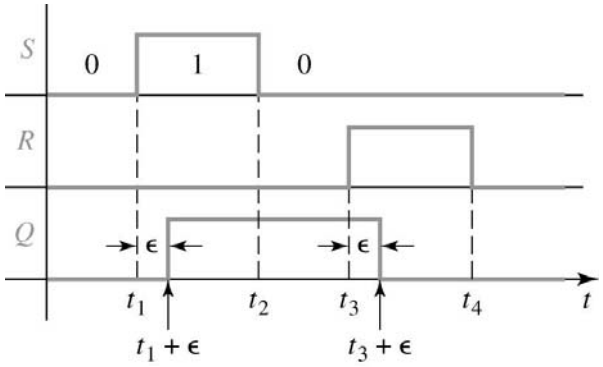
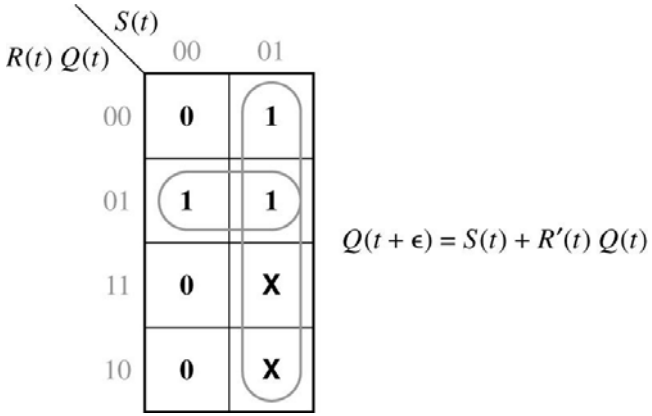


Table 11-1. S-R Latch Operation

$S(t)$	$R(t)$	$Q(t)$	$Q(t+\varepsilon)$	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	–	} Inputs not allowed
1	1	1	–	

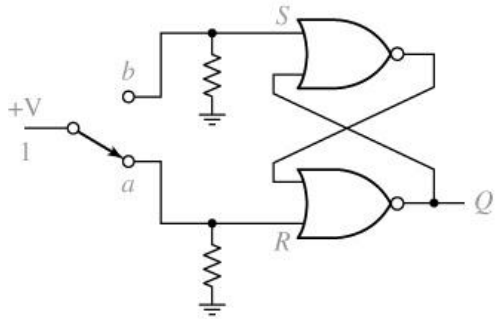
11.2 Set-Reset Latch

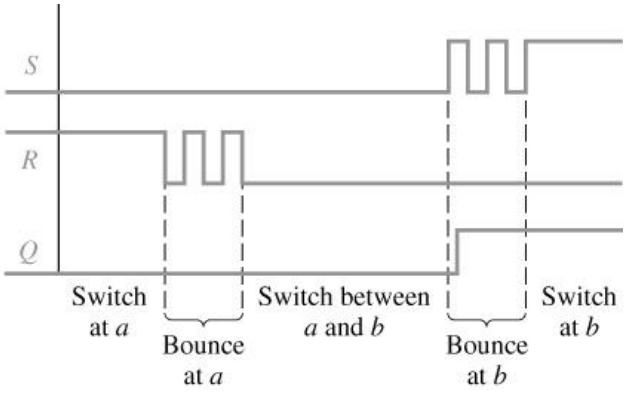
Fig 11-8. Map for $Q(t+\varepsilon)$



$Q(t+\epsilon) = S(t) + R'(t)\,Q(t)$ ⟶ $Q^{+} = S + R'Q \qquad (SR = 0)$

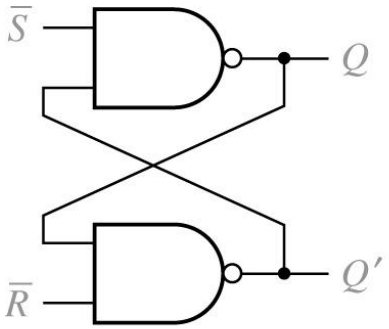
Fig 11-9. Switch Debouncing with an S-R Latch



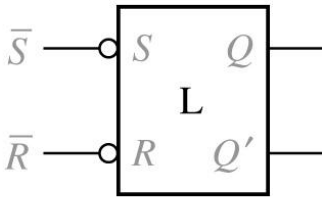


11.2 Set-Reset Latch

Fig 11-10. $\overline{S}$ -$\overline{R}$ Latch



(a)



(b)

S	R	Q	Q^+	
1	1	0	0	
1	1	1	1	
1	0	0	0	
1	0	1	0	
0	1	0	1	
0	1	1	1	
0	0	0	–	} Inputs not allowed
0	0	1	–	

(c)

11.3 Gated D Latch

Figure 11-11. Gated D Latch

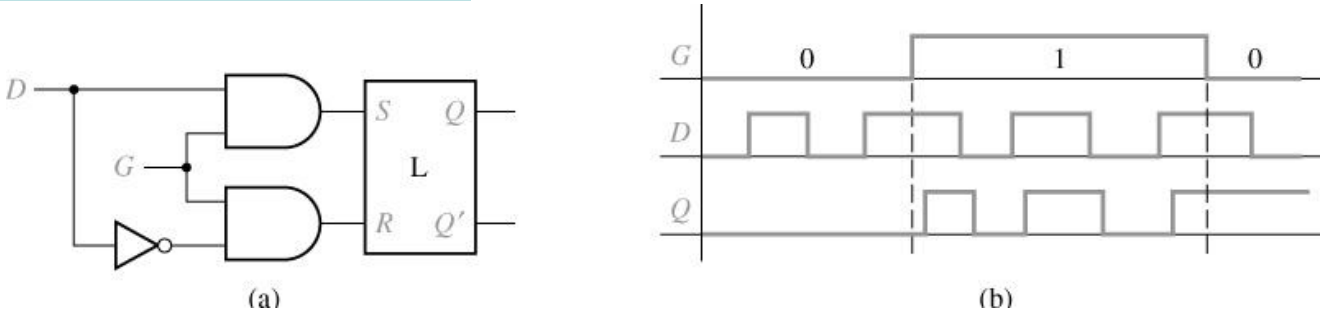
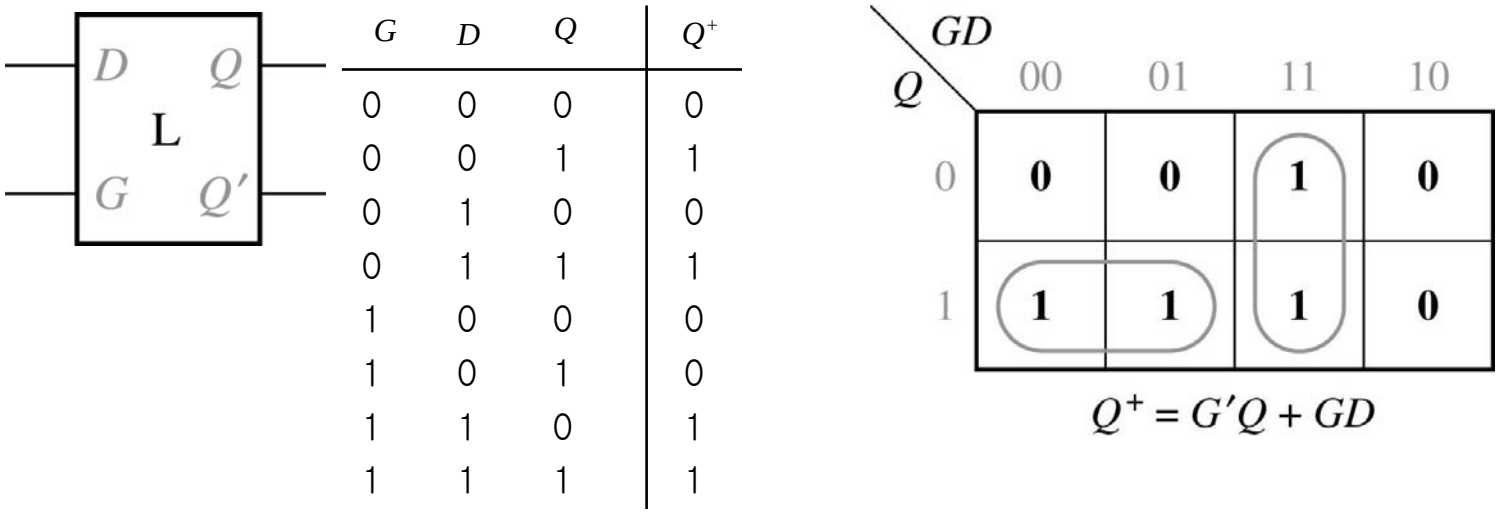


Figure 11-12. Symbol and Truth Table for Gated Latch

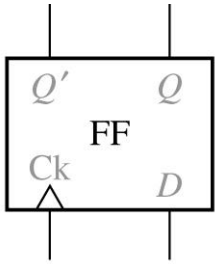


G	D	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

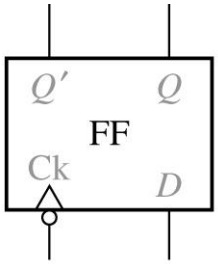
$Q^+ = G'Q + GD$

11.4 Edge-Triggered D Flip-Flop

Figure 11-13. D Flip-Flops



(a) Rising-edge trigger



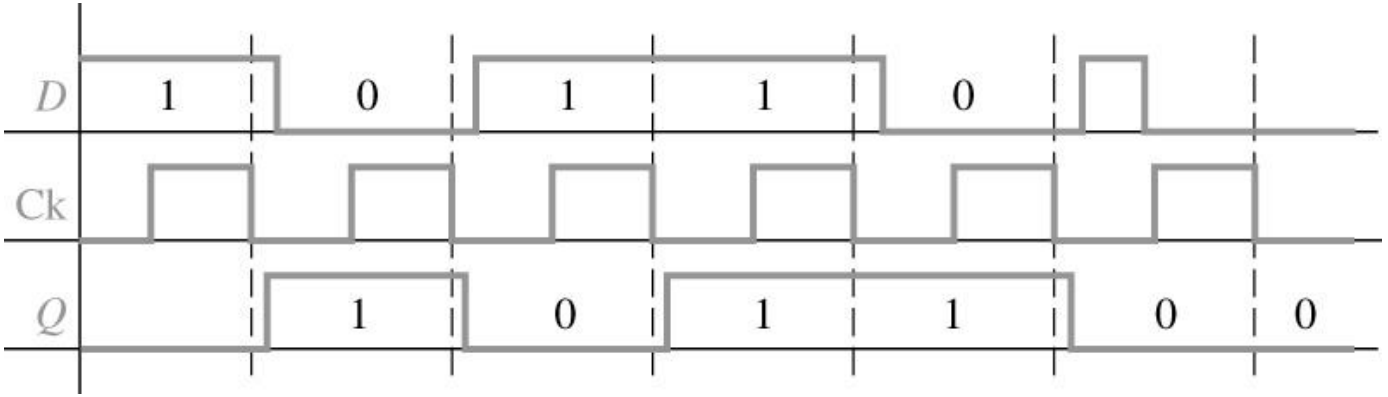
(b) Falling-edge trigger

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

(c) Truth table

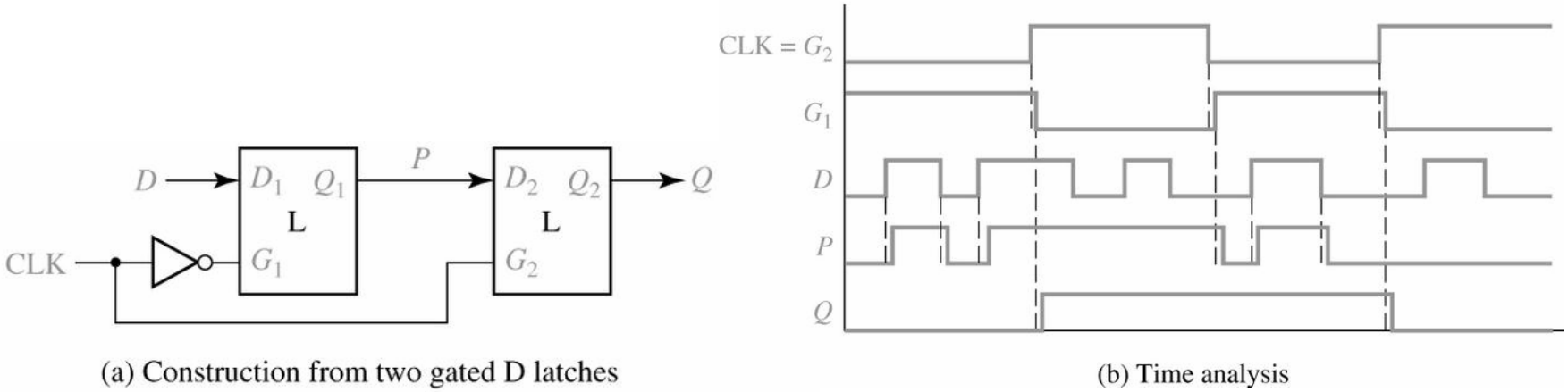
$$Q^+ = D$$

Figure 11-14. Timing for D Flip-Flop (Falling-Edge Trigger)



11.4 Edge-Triggered D Flip-Flop

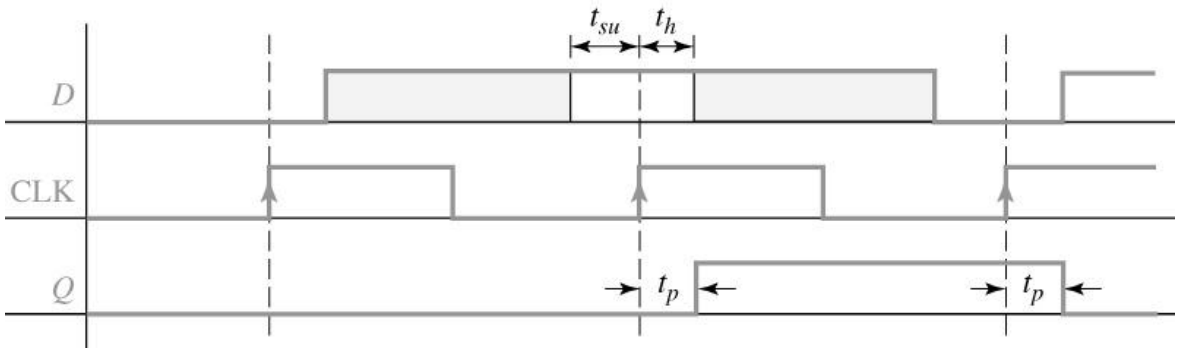
Figure 11-15. D Flip-Flop (Rising-Edge Trigger)



(a) Construction from two gated D latches

(b) Time analysis

Figure 11-16. Setup and Hold Times for an Edge-Triggered D Flip-Flop



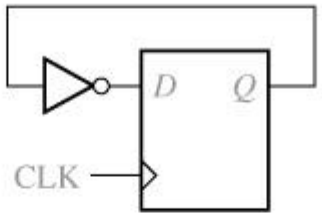
t_{su} : the setup time

t_h : the hold time

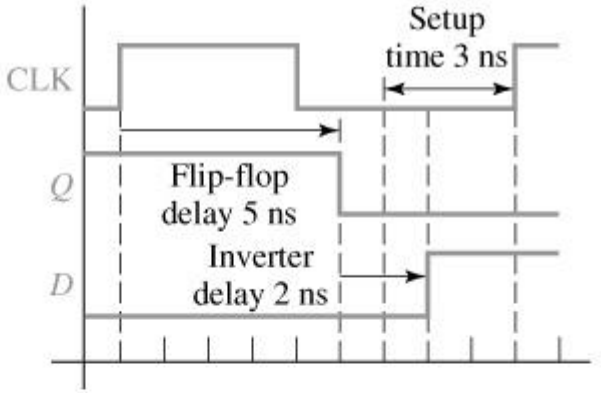
t_p : the propagation delay

11.4 Edge-Triggered D Flip-Flop

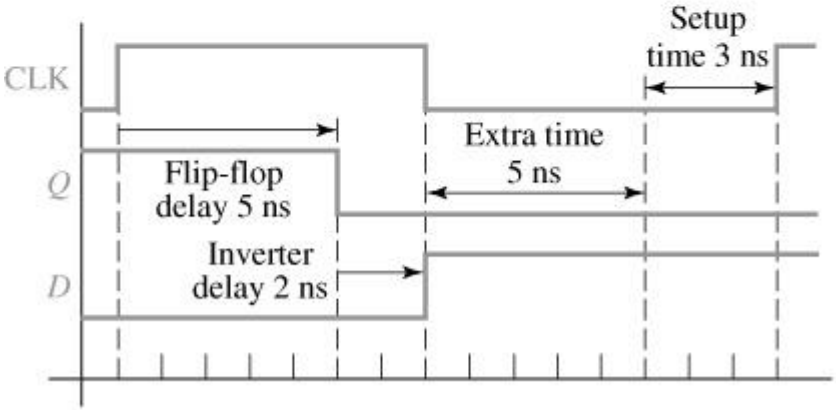
Figure 11-17. Determination of Minimum Clock Period



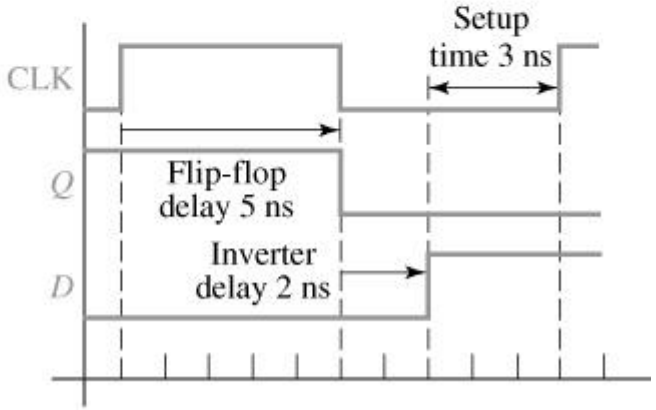
(a) Simple flip-flop circuit



(b) Setup time not satisfied



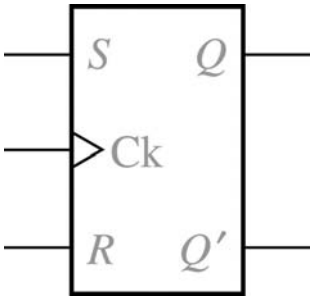
(c) Setup time satisfied



(d) Minimum clock period

11.5 S-R Flip-Flop

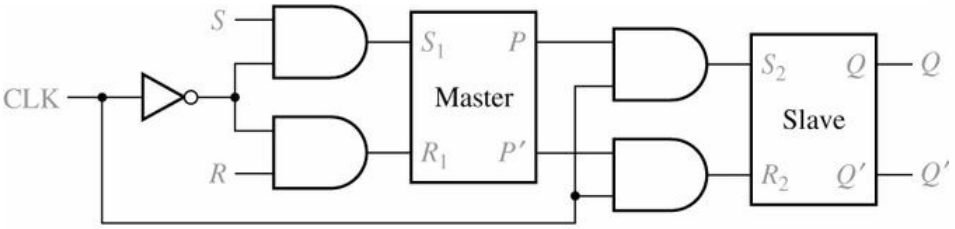
Figure 11-18. S-R Flip-Flop



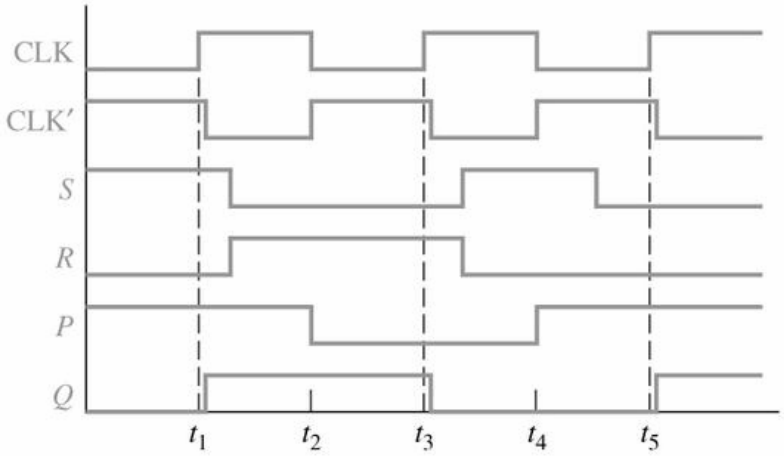
Operation summary :

S=R=0	No state change
S=1, R=0	Set Q to 1 (after active Ck edge)
S=0, R=1	Reset Q to 0 (after active Ck edge)
S=R=1	Not allowed

Figure 11-19. S-R Flip-Flop Implementation and Timing



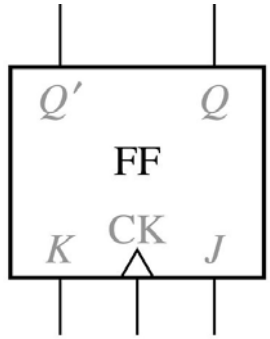
(a) Implementation with two latches



(b) Timing analysis

11.6 J-K Flip-Flop

Figure 11-20. J-K Flip-Flop (Q Changes on the Rising Edge)

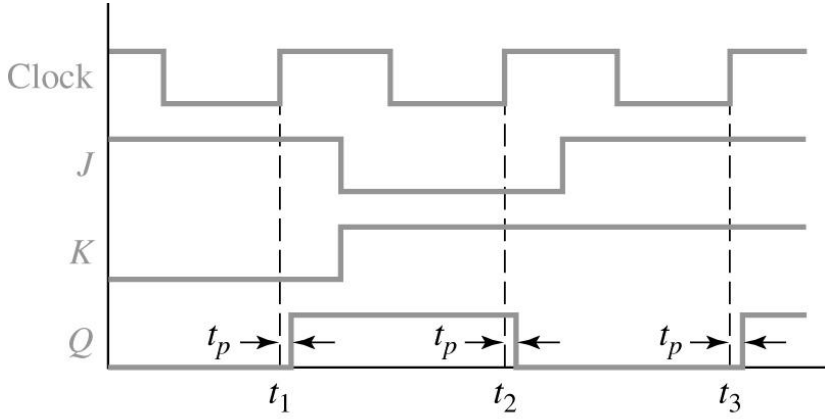


(a) J-K flip-flop

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b) Truth table and characteristic equation

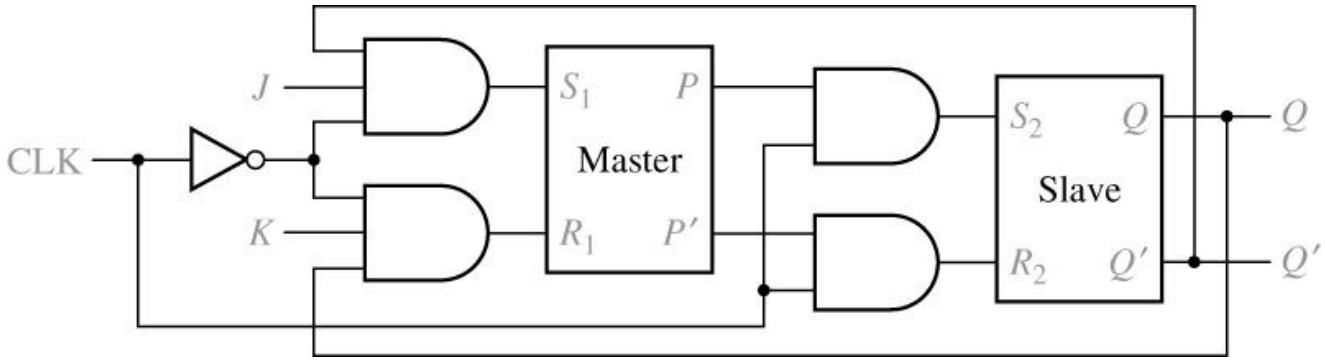
$$Q^+ = JQ' + K'Q$$



(c) J-K flip-flop timing

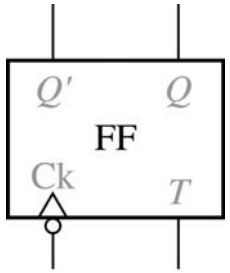
11.6 J-K Flip-Flop

Figure 11-21. Master-Slave J-K Flip-Flop (Q Changes on Rising Edge)



11.7 T Flip-Flop

Figure 11-22. T Flip-Flop



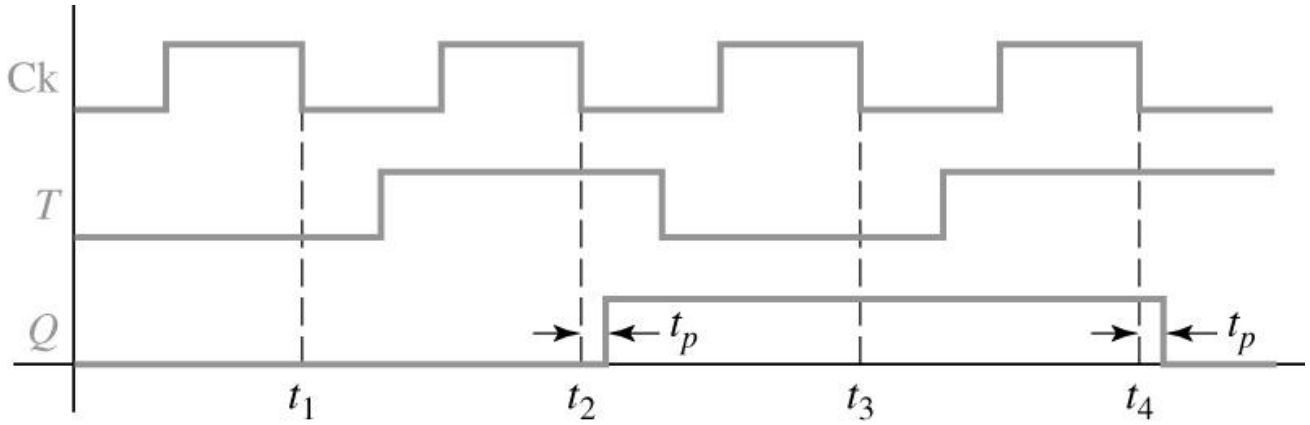
(a)

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

(b)

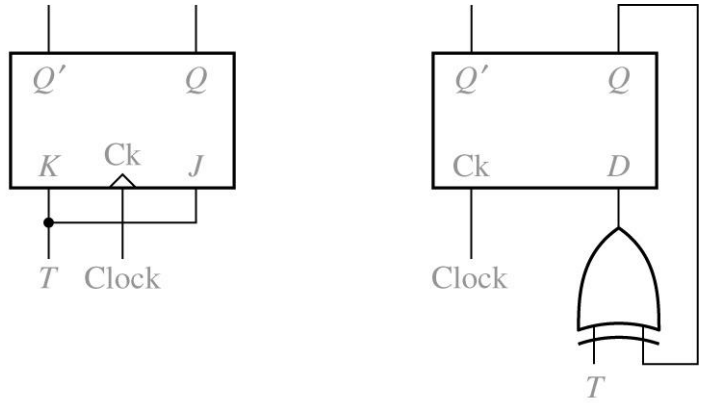
$$Q^+ = T'Q + TQ' = T \oplus Q$$

Figure 11-23. Timing Diagram for T Flip-Flop (Falling-Edge Trigger)



11.7 T Flip-Flop

Figure 11-24. Implementation of T Flip-Flop

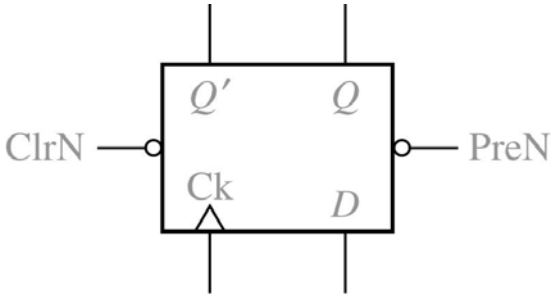


(a) Conversion of J-K to T (b) Conversion of D to T

$$Q^+ = JQ' + K'Q = TQ' + T'Q$$

11.8 Flip-Flops with Additional Inputs

Figure 11-25. D Flip-Flop with Clear and Preset

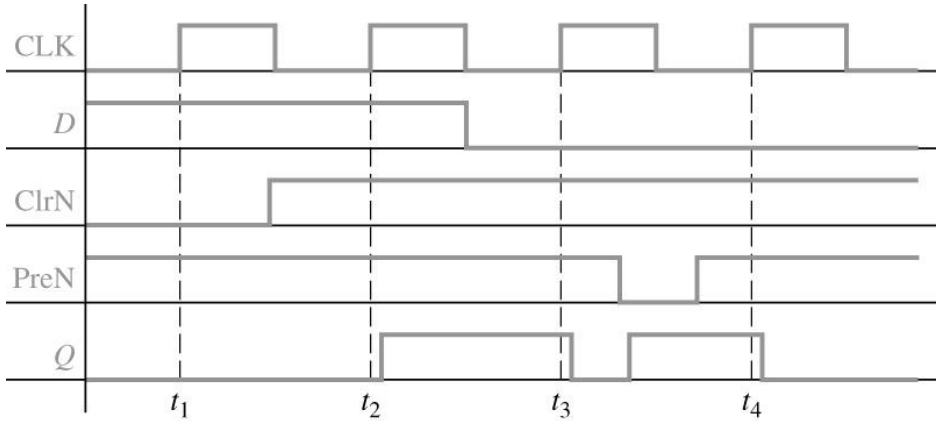


(a)

Ck	*D*	PreN	ClrN	Q^+
x	x	0	0	(not allowed)
x	x	0	1	1
x	x	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0,1,↓	x	1	1	Q(no charge)

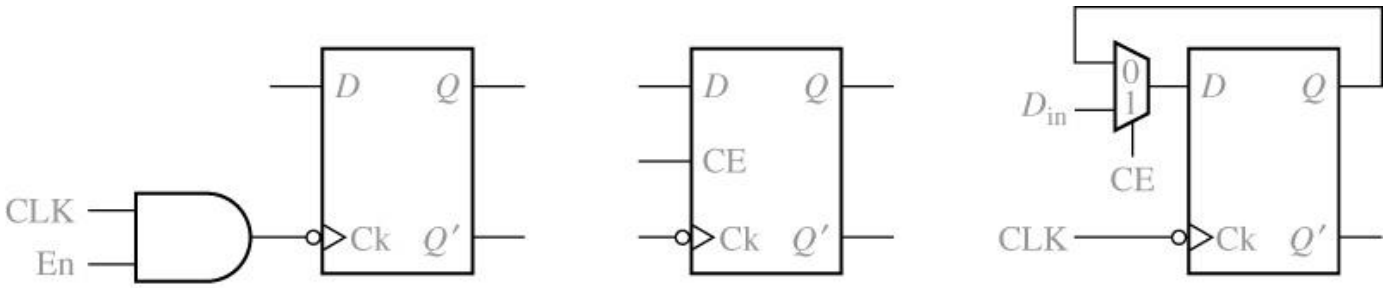
(b)

Figure 11-26. Timing Diagram for D Flip-Flop with Asynchronous Clear and Preset



11.8 Flip-Flops with Additional Inputs

Figure 11-27. D Flip-Flop with Clock Enable



The characteristic equation : $Q^+ = Q \cdot CE' + D \cdot CE$

The MUX output : $Q^+ = D = Q \cdot CE' + D_{in} \cdot CE$

11.9 Summary

$Q^+ = S + R'Q \quad (SR = 0)$ (S-R latch or flip-flop)

$Q^+ = GD + G'Q$ (gated D latch)

$Q^+ = D$ (D flip-flop)

$Q^+ = D \cdot CE + Q \cdot CE'$ (D-CE flip-flop)

$Q^+ = JQ' + K'Q$ (J-K flip-flop)

$Q^+ = T \oplus Q = T'Q + TQ'$ (T flip-flop)