Dual Slope Digital Voltmeter –

The dual slope integrating type DVM integrates the input voltage Vi. The slope of the integrated signal is proportional to the input voltage under measurement. After certain period of time, say t_1t1, the supply of input voltage Vi is stopped, and a negative voltage - Vr of the integrator is applied.
Then the output signal of integrator experiences a negative slope, which is constant and proportional to the magnitude of the input voltage.

The major blocks of a dual slope integrating type DVM are

1. An op-amp employed as an integrator
2. A level comparator
3. Oscillator for generating time pulses
4. Decimal counter
5. Block of logic circuitry

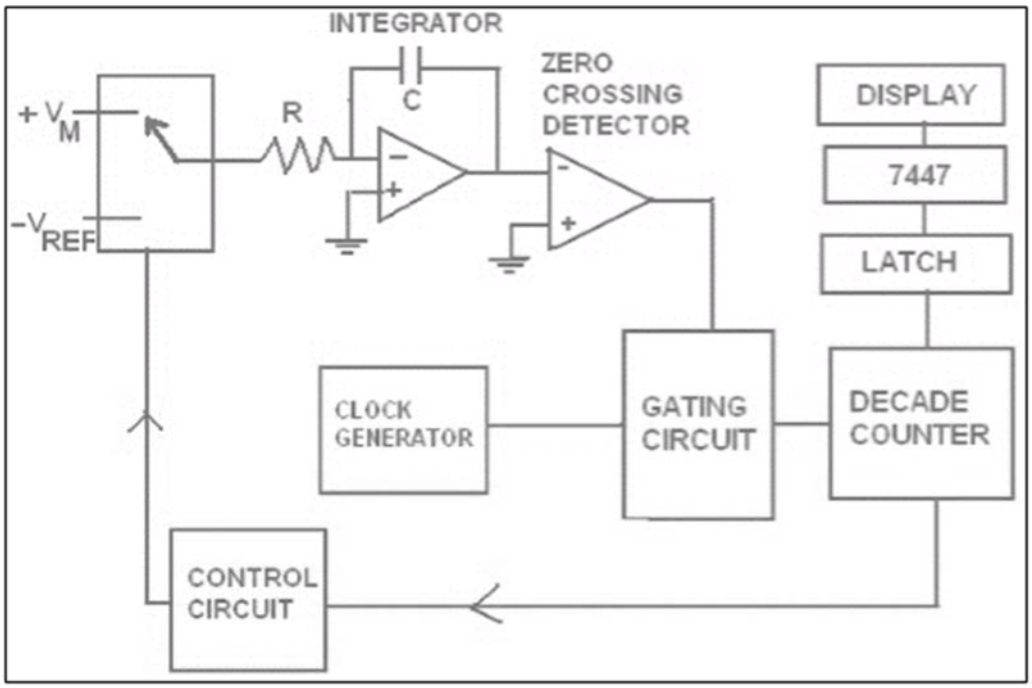

Figure - Block Diagram of Dual Slope DVM

Initially a pulse is applied to reset the counter and the output of flip-flop will be at logic '0.' The switch Sr is in open condition and the switch Si is in closed condition.
Now, the capacitor 'C' starts to charge. Once the output of the integrator becomes greater than zero, the output state of the comparator changes, which in turn opens the AND gate.

When the gate opens, the output of the oscillator (clock pulses) are allowed to pass through it and are applied to the counter. Now the counter counts the number of pulses fed to it. As soon as it reaches its maximum count i.e. that is the counter is preset to run for a time period r; in this condition the maximum count will be'9999', and for the next immediate clock pulse the count changes or goes to '0000' and the flip-flop will be activated.

Therefore, the output of flip flop becomes logic 'I' which in turn activates the switch drive circuitry. This makes the switch Si to open and Sr to close (i.e. the supply of Vi will be stopped, and the supply of V is applied to the integrator.) With this applied signal the output of the integrator will be a constant negative slope i.e. its output signal linearly decreases to zero. This again makes the output of the comparator to change its state which in turn closes the gate.

Here, the discharging time t_2t2 of the capacitor is proportional to the input voltage signal Vi. During this discharging period the counter indicates the count. As soon as, the negative slope reaches zero volts the comparator changes its output state to 'zero' which in turn locks the gate. Once the output of integrator becomes zero (or the input of the comparator is zero) the counter will be stopped and the counted pulses are displayed (which directly gives the input voltage).