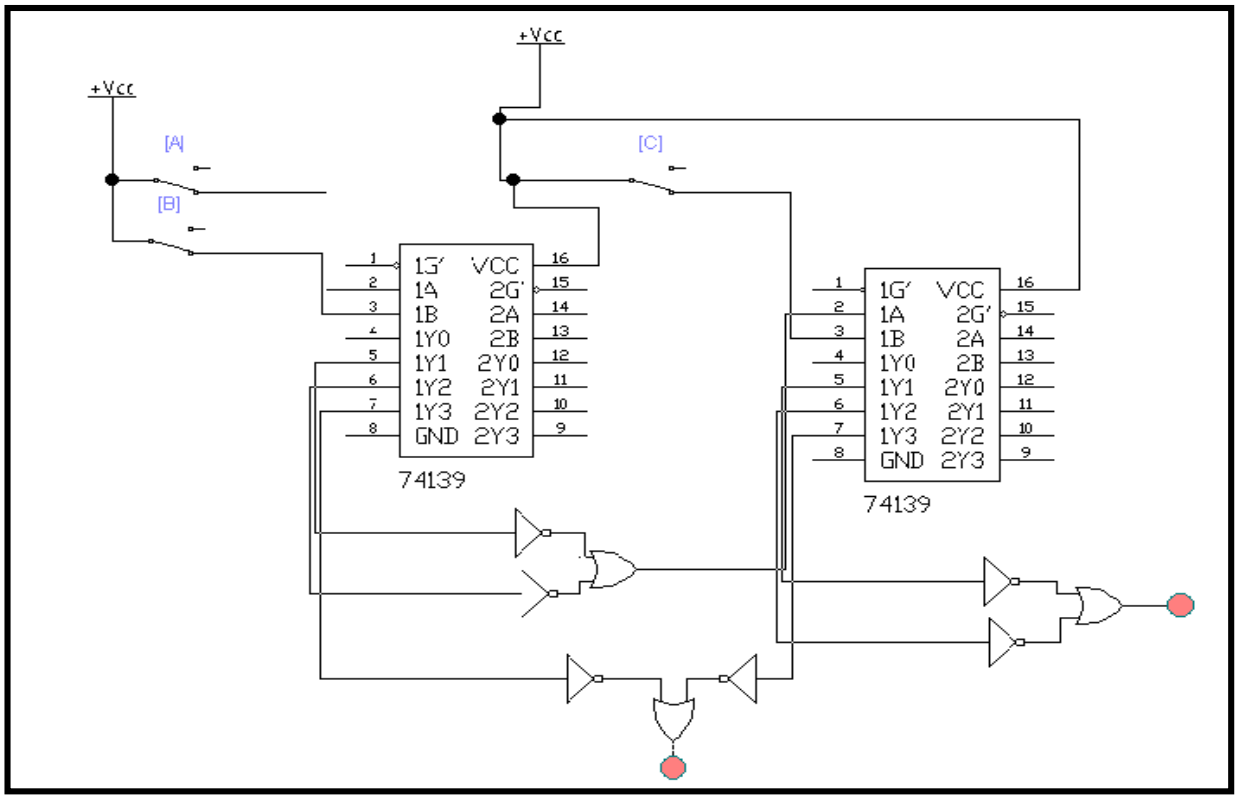
Example :Desgin Full-adder from two (74139) decoder.



1- Encoders

An Encoder is a digital circuit that perform the inverse operation of a decoder . An encoder has 2^n (or fewer) input and n output lines.

The output lines generate the binary code corsponding to the input value. One of the most common Decoders is **(4 to 2)** encoder.The encoder in this system must translate the decimal input signals to binary output signals.

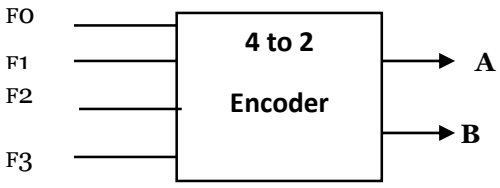
Inputs				Outputs	
F0	**F1**	**F2**	**F3**	**A**	**B**
1	**0**	**0**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**	**1**

0	0	1	0	1	0
0	0	0	1	1	1

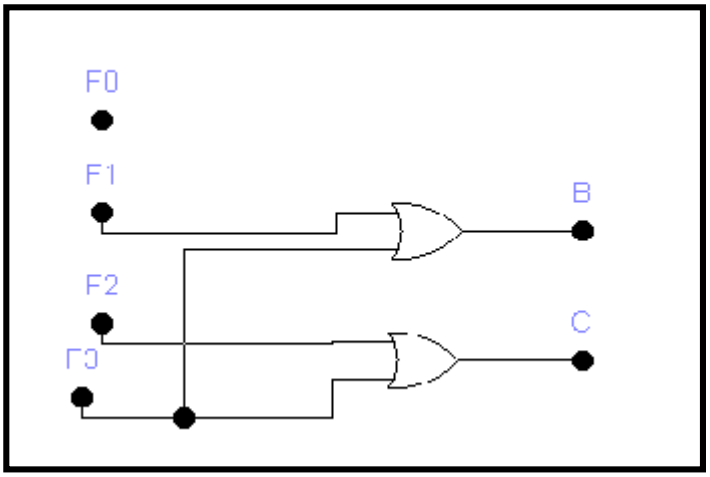
Truth table Of (4-2) Encoder

The truth table is the origin of most logic circuit you must have al the combinations that generate a logic 1 in the truth table, therefore

A=F2 + F3 , B=F1 + F3



Block Diagram Of Encoder



Logic Diagram of Encoder

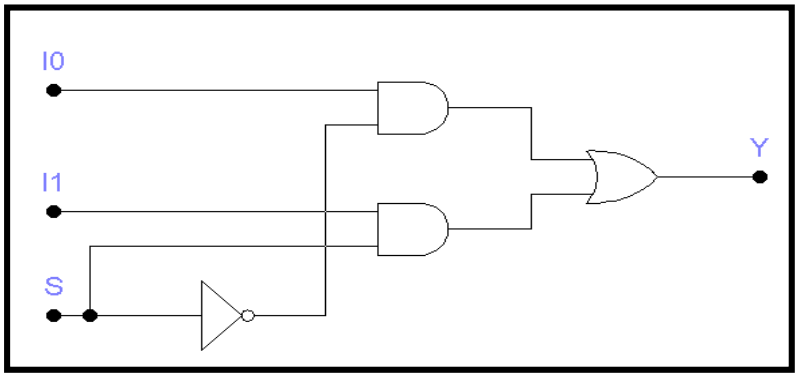
2- Multiplexers

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.

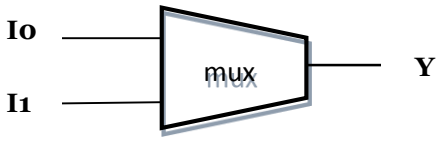
The selection of a particular input line is controlled by a set of selection lines. Normally , there are 2^n inputs and **n** selection lines whose bit combination determine which input is selected and **1** output.

♦ 2 – to- 1 Line multiplexer

A 2 to 1 multiplexer connects one of two sources to a common destination as shown in figure below:



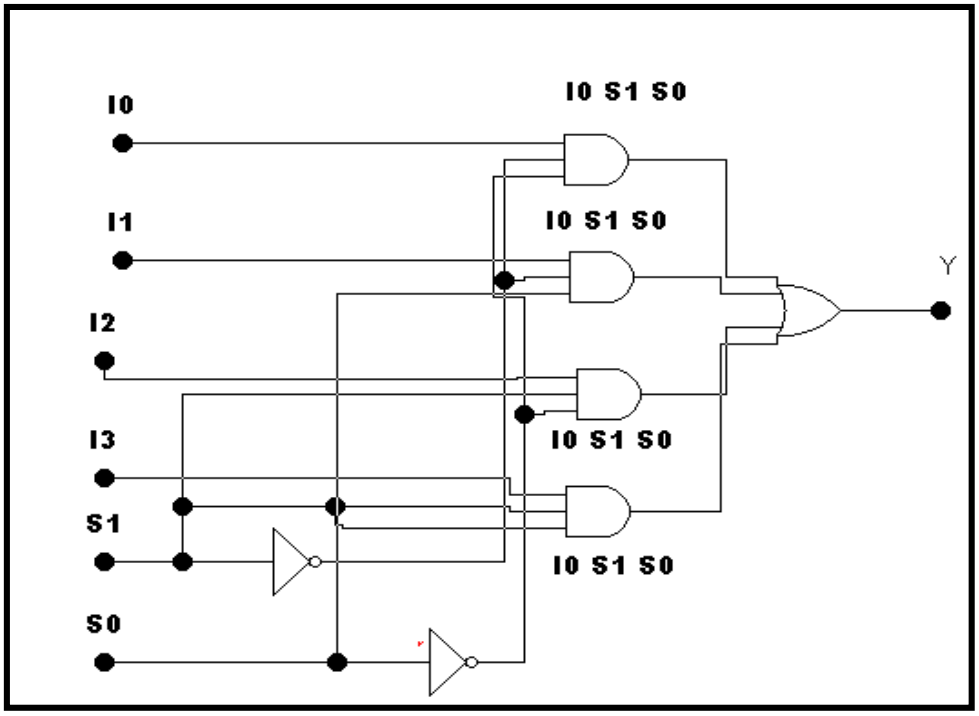
the block diagram of 2-to-1 multiplexer can be shown fellow :



The circuit has two data input lines, one output line, and one selection line **S**.

When **S=0** , the upper **AND** gate is enabled and I0 has a path to the output. When **S=1** the lower **AND** gate is enabled and I1 has a path to the output. The multiplexer acts like an electronic switch that selects one of two sources.

♦ 4 – to - 1 Line multiplexer

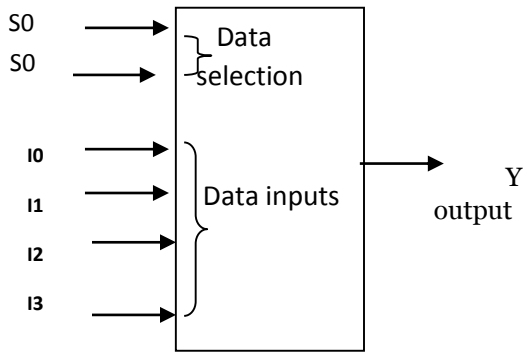


S1	S2	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

- Each of the four inputs , **Io** through **I3** , is applied to one input of an **AND** gate . selection lines **S1** and **So** are decoded to select a particular AND gate.
- The outputs of the **AND** gates are applied to a single **OR** gate that provides the **1-line output**.
- The function table lists the input that passed to the output for each combination of the binary selection values .
- To demonstrate the circuit operation , consider the case when s1s0=10. The AND gate associated with input I2 has two of its input equal to 1 And the third input connected to I2 has the other three AND

gates have at least one input equal to 0, which makes their outputs equal to 0.

- The OR gat output is now equal to the value of I2 , providing a path from the selected input to the output.
- A multiplexer is also called **data selector**, since is selects one of many inputs and steers the binary information to the output line.
- The AND gates and inverters in the multiplexer resemble a decoder circuit and indeed they decode the selection input lines.
- In general **2^n-to-1 line** multiplexers constructed from an **2^n** input lines , one to each AND gate.
- The outputs of the AND gates are applied to a single OR gate.
- The size of a multiplexer is specified by the number **2^n** of its data input lines and the single output line.
- The **n** selection lines are implied from **2^n** data lines.
- As in decoders, multiplexers may have an enable input to control the operation of the unit . when the enable input is in the in active state, the outputs are disabled , and when it is in the active state , thr circuit functions as a normal multiplexer**.**



When (S0=0 and S1=0) the output Y will be I0

And if (So=1 and S1=0) → y= I1

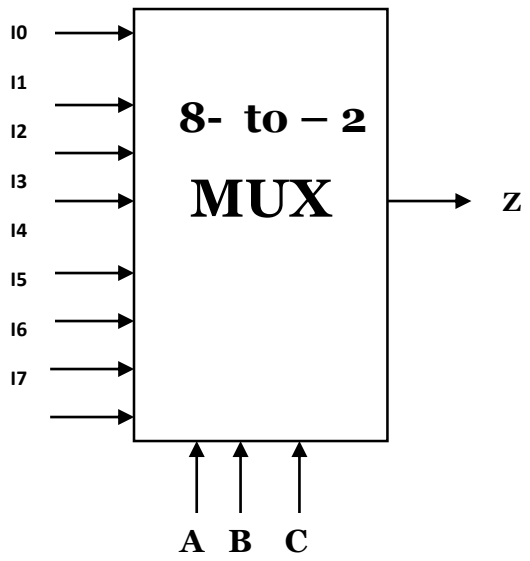
And if (So=1 and S1=1) → y= I2

And if (So=1 and S1=1) → y= I3

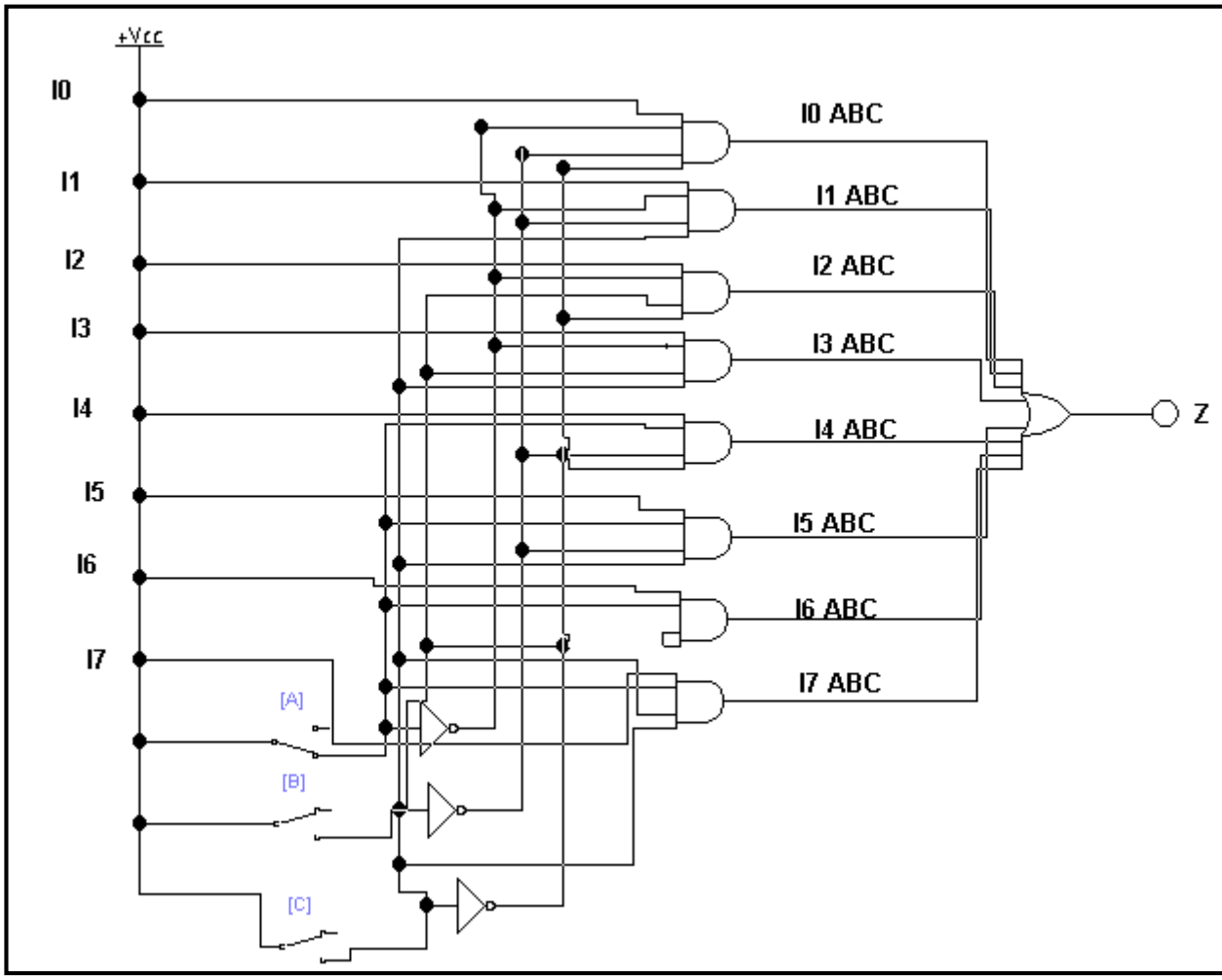
Data inputs	Data Selected		Output
	S1	So	Y
Io	0	0	$I_0 \rightarrow \overline{S1}\,\overline{S0}$
I1	0	1	$I_1 \rightarrow \overline{S1}S0$
I2	1	0	$I_0 \rightarrow S1\overline{S0}$
I3	1	1	$I_0 \rightarrow S1S0$

Selection lines(s1) and (so) are decoded to select a particular AND gate. The outputs of the AND gates are applied to a single OR gates that provide the (1-line) output.

♦ 8 – to - 1 Line multiplexer



An 8-to-1 Mux can be used to realize any 4-variable function with no added gates. Three of variable are used as control inputs to Mux and the remaining variable is used as required on the data inputs.



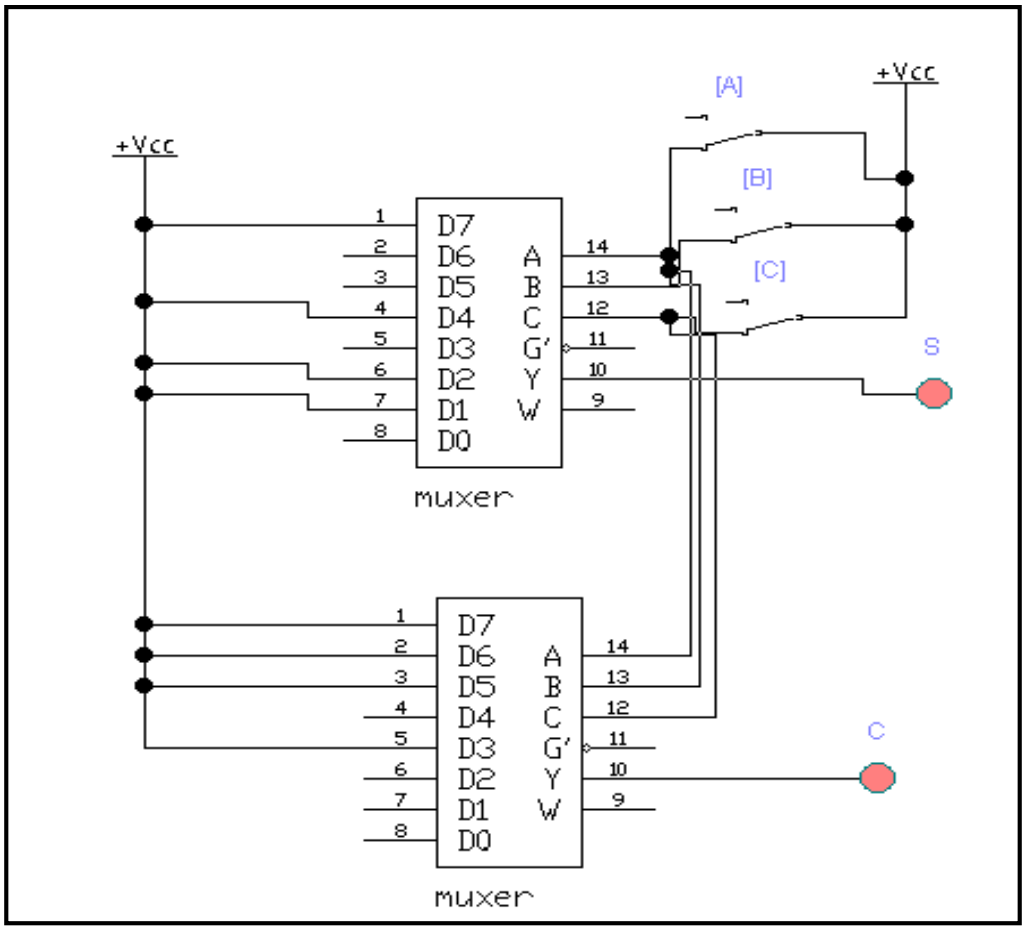
Data Inputs	Data Selected			Output
	A	B	C	
I_0	0	0	0	I_0
I_1	0	0	1	I_1
I_2	0	1	0	I_2

I_3	0	1	1	I_3
I_4	1	0	0	I_4
I_5	1	0	1	I_5
I_6	1	1	0	I_6
I_7	1	1	1	I_7

<u>Example1</u>: using (8*1) multiplexer to realize full adder

from truth table

inputs			output		
A	**B**	**C_{in}**	**$\sum(s)$**	**C_o**	**Decimal NO.**
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	1	0	2
0	1	1	0	1	3
1	0	0	1	0	4
1	0	1	0	1	5
1	1	0	0	1	6
1	1	1	1	1	7
A + B + C_{in}			**Sum**	**Carry out**	

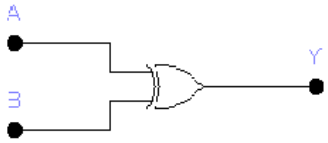


1. *first we have 2^3 inputs =8*
2. *then we have n=3 selection line to each mux*
3. *one output*
4. *full adder need 2 outputs sum and carry then we must connect two mux.*

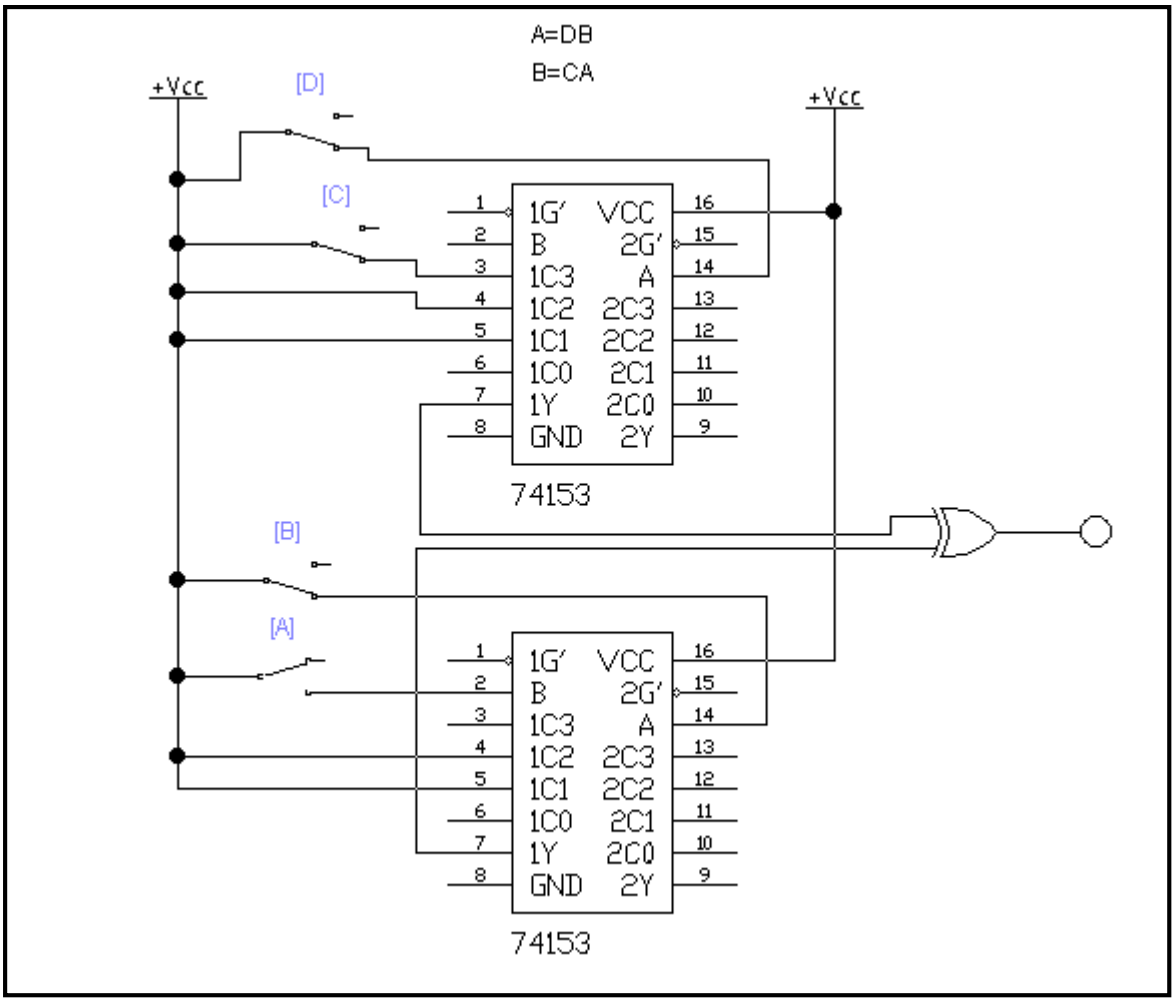
<u>Example2:</u> Design A<>B comparator by using Multiplexers when A, B consist of two digits(N=2) ? hint (use 74153 Mux)

Answer

A <> B ⇔ XOR Gates



Decimal	Bo	Ao	y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

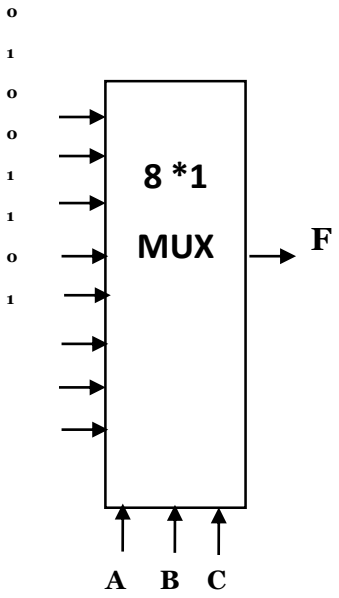


<u>Example3</u>: using multiplexer to realize the switching function

F(A , B , C)= $\sum(1,4,5,7)$

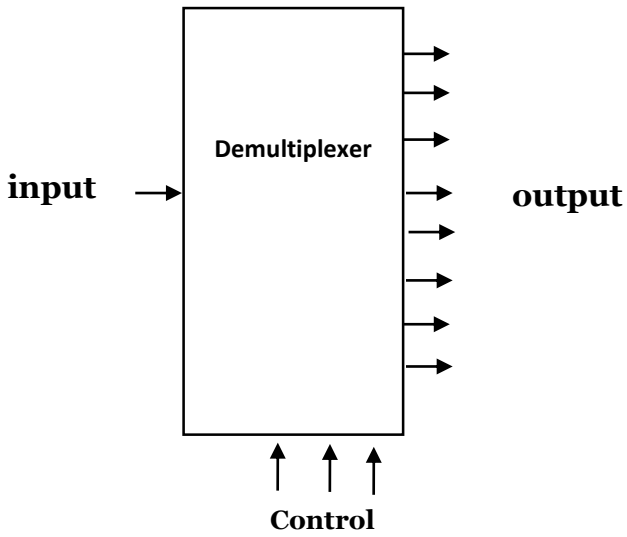
Decimal	A	B	C	Y
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1

5	**1**	**0**	**1**	**1**
6	**1**	**1**	**0**	**0**
7	**1**	**1**	**1**	**1**



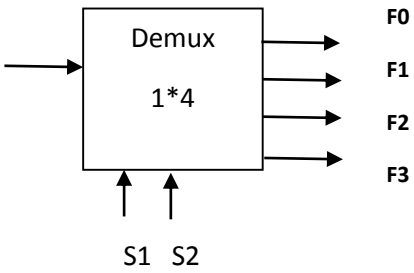
3- Demultiplexer

Is a combinational circuit that perform the inverse operation of Mux

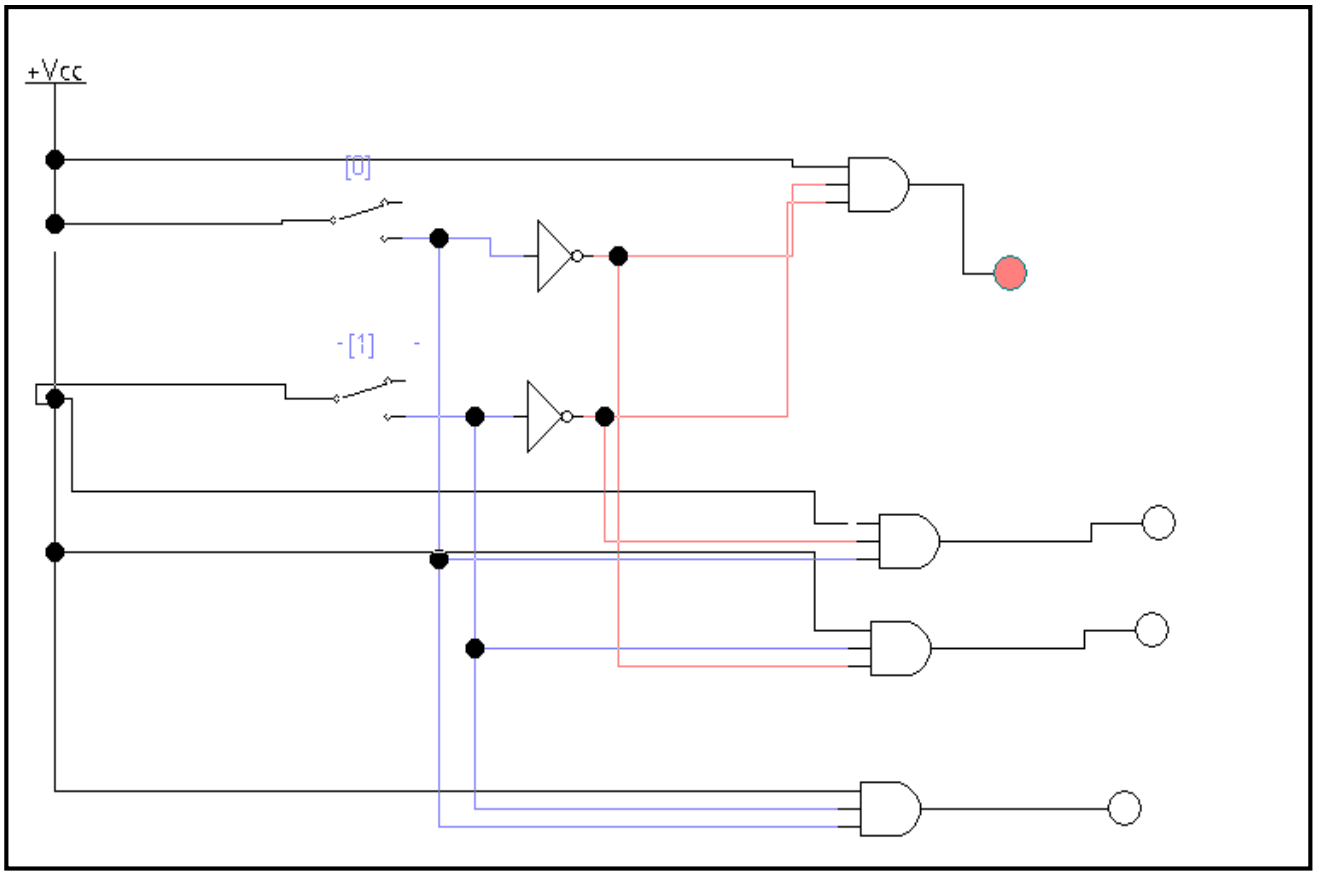


It has one input and 2^n outputs and **n** control lines. The uses of demux is less than the mux circuit in electronics world .

Example : design (1 * 4) Demux



S1	So	output
0	0	F0
0	1	F1
1	0	F2
1	1	F3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